PRACTICAL NANO-MECHANICAL DEVICES FOR ELECTRONIC APPLICATIONS

A Dissertation

Presented to the Faculty of the Graduate School

of Cornell University

In Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

by

Joshua Mark Rubin

January 2014

PRACTICAL NANO-MECHANICAL DEVICES FOR ELECTRONIC APPLICATIONS

Joshua Mark Rubin, Ph.D.
Cornell University, 2014

The increasing difficulty in the scaling of Complementary Metal Oxide Semiconductor (CMOS) devices has given rise to a corresponding increase in the interest of alternate and novel approaches to switching at the nanoscale. Reducing critical dimensions of nanoscale devices has resulted in highly non-ideal switch performance and greater variability of switch characteristics within an ensemble of devices. Solutions to these difficulties have led to an immense increase in complexity of CMOS design and fabrication.

The challenges posed by further size reduction stem from large scale and small scale effects. At the small scale we have quantum effects, and stochastic effects arising from discreteness and noise, and the large scale has thermodynamic issues of large numbers of devices. Two key features of CMOS have seen diminishing returns at the nanoscale: threshold voltage and leakage currents. Smaller devices are less efficient individually and are more difficult to control the on/off switching behavior. Additionally, variability amongst smaller devices has increased the likelihood of device failure or operation outside acceptable design rules. For instance, line edge roughness of optical lithography and dopant fluctuation of implantation have been large sources of inconsistency in fabrication. Therefore, fundamental challenges lie in further scaling, whether through physical laws or material difficulties. And although smaller devices have improved density and speed of integrated circuits, the power density has also increased; whereby thermal management has become a primary difficulty. This myriad of problems is a natural manifestation of more than four decades of device improvement based solely on the enhancement of standard silicon CMOS technology. It is inevitable that silicon technology will hit an ultimate size limit, and being that silicon is still host to the best combination and balance of electronic, mechanical, and material properties, there is great incentive in finding a means to reach the ultimate scalability of silicon.

Two approaches are considered for continuing scaling; increasing functionality of CMOS by heterogeneous integration of other technologies, or a paradigm shift away from CMOS. At this

point there is no other clear alternative. And with a mature silicon technology, it can be extremely advantageous to incorporate suitable alternate technologies with CMOS to enable further scaling.

NanoElectroMechanical Systems (NEMS) of the electrostatic variety have two great advantages to CMOS: zero current leakage and zero subthreshold swing. Although electromechanical switches have been previously suggested for logic, memory, and reconfigurable applications, all previous approaches have utilized either a top down planar approach, or a bottom up vertical approach. Planar approaches suffer from area constraints do to the bending stiffness of the mechanical element. And vertical approaches are limited by variability in growth based structures and other non-CMOS compatible processes. We suggest a new device structure that merges the best of both approaches to create the first top down vertical device. This structure enables the ultimate scalability of NEMS devices and opens the door to potential integration with CMOS via 3D integration. The simple single step lithography fabrication can enable a mechanical device on the scale of CMOS to be useful for error correction; faults and defects inherent to the final nodes of CMOS technology can be potentially rerouted and removed from the signal path, thereby retaining functionality of the greater system.

BIOGRAPHICAL SKETCH

Joshua M. Rubin received a B.S. in Physics from Brandeis University, Waltham, Massachusetts, in 2005. In the same year he received a B.S. in Electrical Engineering from Columbia University, New York, New York through a joint program. During the summers of 2003 and 2004 he worked on compound semiconductor Schottky diode and LED research and development at Emcore Corporation, Somerset, New Jersey. Following his undergraduate studies, he immediately started his Ph.D. studies in the School of Electrical and Computer Engineering at Cornell University under Professor Sandip Tiwari; he also took on a minor in Applied Physics. In 2011 he studied Talmudic logic and reasoning at Mayanot Institute, Jerusalem, Israel. He returned at the beginning of 2012 to complete his Ph.D. studies in 2013. His research interests include design, fabrication, and testing of micro- and nano-mechanical systems including devices based on shape-memory alloys, polymers, semiconductors, and metals. Further interests include semiconductor electronics such as complementary metal oxide semiconductor devices, carbon nanotube electronics, and compound semiconductor devices.

In loving memory of my father Saul S. Rubin

and brother-in-law Noam Lakser,

of blessed memory,

who both passed away unexpectedly

during my graduate studies

ACKNOWLEDGEMENTS

I am extremely grateful for the many wonderful people that I have interacted with and known throughout my time leading up to my Ph.D. and during my graduate studies. I am honored to have exceptional family, friends, and colleagues, and I have gained so much from them. Those around me have added to my life immeasurably in terms of inspiration, friendship, and insight. And I am humbled by the many kindnesses that they have shown me time and again.

I would like to thank Professor Sandip Tiwari for the guidance, support, and patience that he has offered me. I respect him greatly as a researcher and as a person. He has genuine concern for his students and regularly displays his care for each person as a whole and multifaceted individual. His curiosity and perceptiveness sparked deeper and more penetrating areas of research within my own work, and his willingness to let me explore allowed me further development as a scientist.

I would also like to thank my committee members, Professor Paul McEuen and Professor Robert Buhrman. I am very grateful for their interest and willingness to be involved with my graduate work. I would also like to thank Professor Amit Lal for sharing his group's facilities and resources. I have learned much from interacting with his many exceptional students. In particular, I have been fortunate to work alongside Kwame Amponsah, Siva Pulla, and Shankar Radhakrishnan. Furthermore, I am grateful for the friendship and guidance of Serhan Ardanuc, who at times felt like a postdoc to Professor Tiwari's research group.

I am thankful for the members of Professor Tiwari's research group, past and present. I have enjoyed the companionship and insights of: Moon-Kyung Kim, Sang Hyeon Lee, Jae-Yoon Kim, Wei Min Chan, Arvind Kumar, Helena Silva, Ali Gokirmak, Chris Liu, and Kevin Kim. I am especially grateful for my interaction with Brian Bryce; I have gained much from his knowledge and insights. I am thoroughly grateful for Ravishankar Sundararaman, whose impressive theoretical abilities helped support and guide my work during a very critical time. I must truly thank him for helping develop the analytical models for the devices in my dissertation. I am also appreciative to have had a kind and enjoyable officemate, Marcus Gingerich.

I am also grateful for the many facilities and resources that I used during my Ph.D. I would like to thank the staff of the Cornell Nanoscale Facility (CNF), Cornell Center for Materials Research, and Center for Nanoscale Systems. I would also like to thank the staff at the Harvard Center for Nanoscale Systems. I am particularly grateful for the advice and technical support that I have received from Merideth Metzler, Gary Bordonaro, and Noah Clay. Furthermore, one particular CNF user, Gregory Simelgor, helped shape and guide my approach to nanofabrication at the very beginning of my time at Cornell. I must also thank the funding agencies that have supported me: National Science Foundation under grant 1128518, Cornell Center for Nanoscale Systems, NYSTAR, and Samsung.

I would also like to thank the friends that I have enjoyed the company of while in Ithaca, NY: Steven Gordon, Gabriel Goldenberg, Joshua Bleznick, Ian Taylor, Sol Hart, Ezekiel Finn, Alex Damianou, Evan Schwartz, Yoav Linzon, and Ben Sacks. This list is not all inclusive.

I would like to specially thank my dear family members. I thank my Mother for supporting me through numerous challenges that I faced during my graduate work and regularly looking over my well-being. And I thank my sisters, Rachel Rubin, Sarah Lakser, Jessica Weiss, and Shaindel Scott also for their support and love. I am also grateful to their husbands for their friendship and for being the "brothers" I never had. I am especially thankful for my Father, of blessed memory, who always lent me an ear, no matter what time of day or night. And of my family, I truly want to thank my wife, Chaya-Bracha Rubin, who I met in Ithaca during my graduate studies. Her support, positivity, love, and willingness to embark on the journey of life with me, has enhanced my life and been a resource of tremendous personal growth.

Finally, I would like to thank the Rabbis that I have interacted with during my time at Cornell. Rabbi Eli Silberstein has been like a father to me, and also a tremendous friend. Without his guidance and support I would not have been able to finish my graduate work, nor would I have met my wife. He has guided me through numerous challenges common to life, and I have learned much from his brilliance. I would like to thank Rabbi Shlomo Rothstein and Rabbi Dovid Birk for their friendship, inspiration, and counsel. And I would also like to extend special appreciation to Rabbi Betzalel Broh, who has shown me what true friendship means. Lastly, I would like to thank the Lubavitcher Rebbe for his incredible inspiration and wisdom, and for having the insight and will to send Chabad Rabbis throughout the world to serve as emissaries and sources of inspiration. To conclude, I would like to thank G-d, Who continues to enliven me, sustain me, and Who has brought me to this moment.

TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 SCALING OF CMOS

The phenomenal success of silicon MOSFET (metal-oxide-semiconductor field-effect transistors) scaling over more than half a century has to lead to increasingly more fundamental challenges to further size reduction. These difficulties can be subdivided into two general categories that encompass a change of scale from the nano to the macro, with quantum effects and other probabilistic phenomena influencing and determining device performance at small scales, and thermodynamic consequences and limitations for large scale integration establishing the ultimate usage of nanoscale devices [1]. Silicon technology faces particular challenges from increasing power density, variability, and reliability. Reduction in size of nanoscale transistors has resulted in diminishing returns. Quantum mechanical effects have caused leakage currents (I_{OFF}) to increase and threshold voltages (V_T) to stop scaling. Additionally, the cost in energy consumption per digital logic gate has also stopped scaling due to the increase in probabilistic variation [2]. Therefore, although device size has truly scaled, the overall trend is towards increasing power density, whereby inefficiencies at the device level give rise to difficulties at larger scales.

Numerous approaches have been taken to overcome the obstacles present in recent generations of silicon technology. At the device level, SOI (silicon on insulator), high-k dielectric and metal gates, double-gates, finfets, and all-around-gates, have been employed to control and mitigate short channel effects. Future devices will most likely incorporate more novel materials for additional performance enhancement. However, silicon will remain an

essential building block while moving forward. Although circuit level changes have also assisted in reducing power consumption, system level changes have effected a much greater change. The two contributions to energy dissipation by CMOS (complementary metal oxide semiconductor) are dynamic energy from charging and discharging capacitors and static energy caused by off-state leakage. Given a long-channel MOSFET in the saturation region, with $V_{DS} \geq V_{GS} - V_T$ and $V_{GS} > V_T$, relevant design parameters for on-current can be expressed as:

$$I_{ON} \propto \mu_{eff} C_{ox} \frac{W}{L} (V_{DD} - V_T)^2 \tag{1.1}$$

With μ_{eff} defined as the effective carrier mobility, C_{ox} as the gate capacitance per unit length, W/L as the ratio of the gate width to the length, and V_{DD} as the supply voltage. Additionally, the off-current is given by:

$$I_{OFF} \propto 10^{-V_T/SS} \tag{1.2}$$

With the $V_{GS} = 0$, and $V_{DS} = V_{DD}$. Where SS is defined as the sub-threshold swing, which is found by taking the inverse slope of the $\log(I_{DS})$-V_{GS} curve. In the sub-threshold region, carrier diffusion increases exponentially as a function of potential barrier height, which is controlled by V_G. For an ideal MOSFET at room temperature, thermal diffusion limits the value of SS to approximately 60 mV/dec.

Therefore, when the supply voltage, V_{DD}, is lowered, dynamic power decreases for a given threshold voltage. However, to maintain drive current, threshold voltage must also be decreased, as is understand from Equation 1.1. Meanwhile, a lower threshold voltage implies a larger leakage current, as seen from Equation 1.2. Other scaling methodologies can also be employed; however, a general tradeoff exists between the on-current and off-current.

A clever solution that furthered microprocessor performance from the system level involved an additional parameter, frequency. Since a minimum total energy point exists for the

dynamic and static power dissipation, operation at that point is most beneficial from an energy standpoint, but not from the perspective of time (frequency). Therefore, parallelism has been successfully employed to operate devices at a lower frequency, i.e. lower energy point, but to run multiple cores in parallel to enhance the overall performance of the system. Ultimately, since a MOSFET has a definitive energy efficiency limit (not withstanding material changes), parallel configurations can only hope to achieve the limit. This is where current technology stands, in search of new device geometries, materials, and replacement CMOS devices for elimination of leakage currents. However, silicon will see out its ultimate scalability if no alternative technology proves to have an outright advantage in terms of time, size, and energy.

1.2 ALTERNATIVE APPROACHES TO COMPUTING

Aside from the developing new materials to be incorporated into CMOS structures (III-V's, Ge, etc.), and new architectures within the realm of CMOS (multi-gate structures), numerous devices are being suggested for CMOS replacement in memory and logic applications. Some of these technologies include: ferroelectric FETs, resistance based two-terminal devices, MIT (metal insulator transition) switches, carbon nanotube FETs, graphene FETs, spin FET, nanowire FETs. Certain technologies excel in particular areas of computation in comparison to silicon. Therefore, although there may not be an absolute replacement for CMOS yet, there is room for novel devices to be either co-integrated with CMOS or heterogeneously integrated via 3D stacking of chips. One such technology that exhibits two key features lacking in MOSFETs are NEMS switches. Although electronic computing superseded mechanical switches ~ 50 years ago [3], ironically, developments in MEMS have led to a revival of interest in mechanical

switches for nano-electronic computation. Nano-mechanical switches offer virtually zero off-state leakage current and zero subthreshold swing. The leakage currents are suppressed by using air gaps for electrical isolation. And zero subthreshold swing is a result of the intrinsic digital nature of the switch, whereby the presence or absence of physical contact determines the on- or off-state of the switch, respectively. Other features of interest include simple fabrication, possibility of fabrication on inexpensive substrates, and potential for 3D integration. CMOS has a strong advantage in speed over mechanical switches, with predictions for switching times limited to ~ 1 ns [4]. However, given the improved energy efficiency of NEMS switches, new nano-mechanical structures with sizes approaching those of CMOS can be seriously considered for heterogeneous integration with CMOS for enhanced CMOS functionality and performance.

1.3 ELECTROSTATIC MEMS/NEMS SWITCHES

Although MEMS/NEMS utilize a vast array of actuation schemes, the four most prevalent methods are electrostatic, piezoelectric, magnetic, and thermal. The most widespread and simplest to fabricate is the electrostatic actuator. Further discussion of these methods will be found in Chapter 2 while discussing scaling of MEMS to NEMS. When a potential is applied across any capacitor (either parallel or fringing), an electrostatic force is exerted on the plates (conductors) in accordance with the charge buildup. Capacitive plates with opposite charge always results in an attractive electrostatic force. If the insulator in the capacitor is replaced by air, and at least one plate is allowed to move, a discernible and useful displacement of the movable electrode is achievable. The electrostatic force at the micro- and nano-scale has been successfully employed in sensors and actuators for the detection of inertial forces and pressure

changes in the form of accelerometers and gyroscopes as well as ultra-sensitive particle detection, optical switches and display devices, and mechanical filters and switches. As mechanical devices move to the nano-scale, the inherent simplicity of electrostatic based devices will lend itself to aggressive scaling and increased utility at scales relevant to CMOS integration.

1.3.1 Principle of Operation

The simplest manifestation of an electrostatic actuator consists of a single set of parallel conductive plates in a two terminal configuration, as shown in Figure 1.1. The electrostatic force on the plates shown in Figure 1.1, with plate area given by *A*, can be derived from the energy stored in a capacitor:

$$E_c(y) = \frac{1}{2}C(y)V^2 = \frac{A\varepsilon_r\varepsilon_o}{2(d-y)}V^2 \tag{1.3}$$

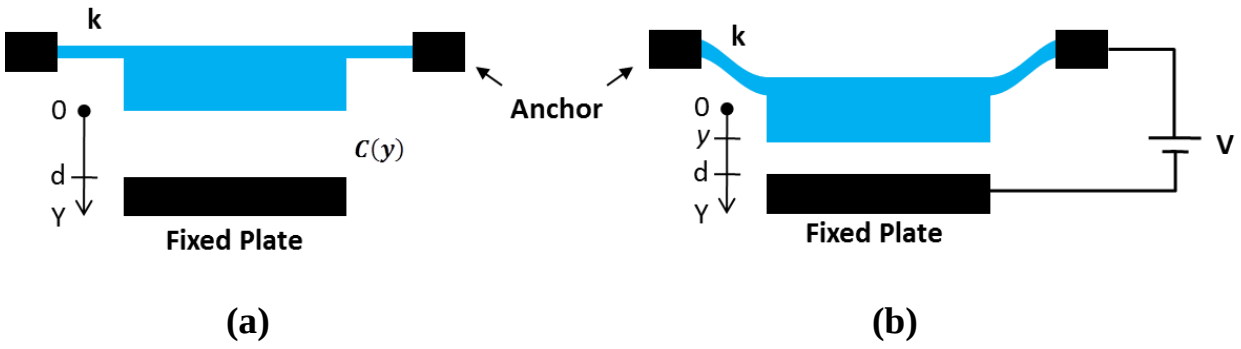


Figure 1.1: Simple parallel plate electrostatic actuator, reproduced from [5]. (a) Schematic of design with one moveable plate and one fixed plate. Moveable plate has flexures with spring constant k, and central plate with increased thickness to simplify modeling to that of a parallel plate configuration. (b) An applied voltage results in a particular displacement, *y*.

The electrostatic force is given by the negative derivative of the capacitive energy with respect to position:

$$F_e = -\frac{\partial E_c(y)}{\partial y} = \frac{A\varepsilon_r\varepsilon_o}{2(d-y)^2}V^2 \tag{1.4}$$

Additionally, the mechanical restoring force on the moveable electrode is given by:

$$F_k = -ky \tag{1.5}$$

If the only two forces acting on the moveable electrode are the electrostatic force and the mechanical restoring force, then the equilibrium condition for force is given by:

$$F = F_e + F_k = 0 \tag{1.6}$$

Therefore, given that the electrostatic force is super-linear (quadratic) and the mechanical restoring force is linear, a condition exists where the electrostatic force exceeds the mechanical restoring force for increasing values of displacement. This point is referred to as the pull-in voltage of the device, V_{PI}, and it also represents the turn on voltage of devices that exhibit this instability. After pull-in, the applied voltage can be lowered while still maintaining contact between the electrodes. At a particular voltage referred to as the pull-out voltage, V_{PO}, the mechanical restoring force will overcome the electrostatic force, and the moveable electrode will abruptly snap out, assuming that adhesion forces do not permanently attach the moveable plate to the fixed plate. Since the electrostatics are much more favorable once the device is pulled-in, pull-in voltage will inevitably be higher than pull-out voltage, thereby making hysteresis intrinsic to electrostatic actuators based on the pull-in condition. This hysteresis can be useful for memory-type applications and will be discussed later on.

1.3.2 Design Considerations

The figures of merit relevant to CMOS design are also key indicators of the performance and benefit of NEMS switches. Operation voltage, switching speed, and reliability as well as on/off-state performance all determine potential value of a given technology. These metrics will also be discussed in reference to nano-mechanical switches.

1.3.2.1 Operation Voltage

By continuing the analysis shown in Section 1.3.1, an expression for pull-in voltage can be determined. Starting with Equation 1.6, and substituting in the expressions for force yields:

$$\frac{A\varepsilon_r\varepsilon_o}{2(d-y)^2}V^2 - ky = 0 \tag{1.7}$$

The mathematical condition for stability requires that $\frac{\partial F}{\partial y} < 0$. Applying this condition to Equation 1.7 and solving for the critical value of *y* at which pull-in occurs gives:

$$y < \frac{d}{3} \tag{1.8}$$

Therefore, for any values of *y* less than a third of the gap, the moveable electrode finds a stable equilibrium point with the electrodes isolated by an air-gap, and the device remains in the off-state. The voltage in Equation 1.7 can then be evaluated for *y = d/3* to find the pull-in voltage:

$$V_{PI} = \sqrt{\frac{8kd^3}{27A\varepsilon_r\varepsilon_o}} \tag{1.9}$$

As mentioned briefly is section 1.3.1, the pull-out voltage can also be determined in a similar fashion based on a simple device configuration shown in Figure 1.2.

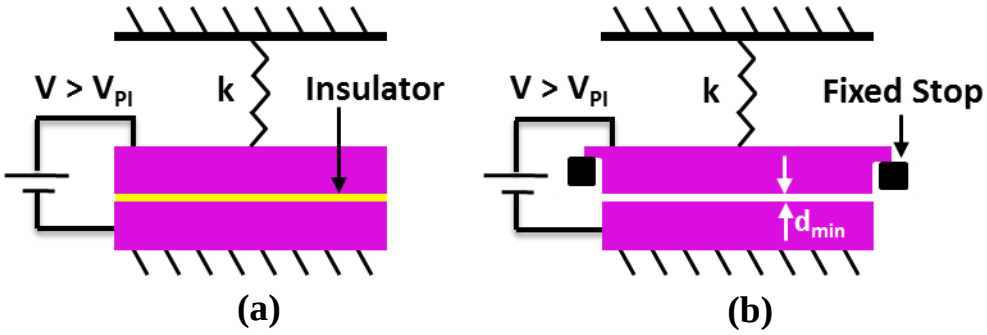


Figure 1.2: Parallel plate structure after pull-in condition reached. (a) Parallel plates separated by a thin insulator to prevent shorting. (b) Moveable electrode contacts fixed stops after pull-in before snapping to bottom electrode, thereby maintain a small gap, d_{min}.

Two simple scenarios shown in Figure 1.2 prevent shorting of the electrodes after pull-in. For a two terminal device, utilizing a thin insulating layer or fixed stops (bumpers) to maintain a small gap, d_{min}, also prevents electrical contact and useful switching behavior. However, for demonstration purposes of pull-out voltage, the designs in Figure 1.2 are useful. Taking into surface adhesion forces, f_a, the mechanical restoring force must overcome the electrostatic force and the surface adhesion forces to achieve pull-out. The equation for force on the moveable electrode once it is contact with the fixed electrode is given by:

$$\frac{A\varepsilon_r\varepsilon_o}{2(d-y)^2}V^2 + f_a = ky \tag{1.10}$$

Setting $y = d - d_{min}$ and solving for the voltage at which the device pulls-out for a given adhesive force results in the expression:

$$V_{PO} = \sqrt{\frac{2d_{min}^2}{A\varepsilon_r\varepsilon_o}[k(d-d_{\min}) - f_a]} \tag{1.11}$$

One additional configuration worth mentioning is the case of contact without pull-in. This can be achieved by choosing the air-gap dimensions and fixed stoppers or contact dimples such that

contact is made before the pull-in condition is achieved. This requires that the stoppers are placed less than a distance of *d/3* from the initial zero-voltage equilibrium position (in this simple parallel plate example). However, this method greatly restricts an actuator's range of motion. Another approach, which will be revisited later in Chapter 3, involves the addition of a series capacitor [6], configured as shown in Figure 1.3. This series capacitor, C_s, is of fixed capacitance and forms a voltage divider with the variable mechanical capacitor, C_m. The effect of C_s is to transform the structure so that the effective gap becomes much larger than the original gap. The original gap of d becomes $d_{eff} = d + d_s/\varepsilon_r$ for the purpose of evaluating the pull-in voltage, as seen in Figure 1.3(b). Therefore, if $d_{eff} > 3d$ then the moveable electrode will make contact with the fixed surface before it reaches the pull-in condition at $d/3$. However, one disadvantage of this technique is the additional voltage drop across the series capacitor. As a result, a significantly higher operation voltage is required.

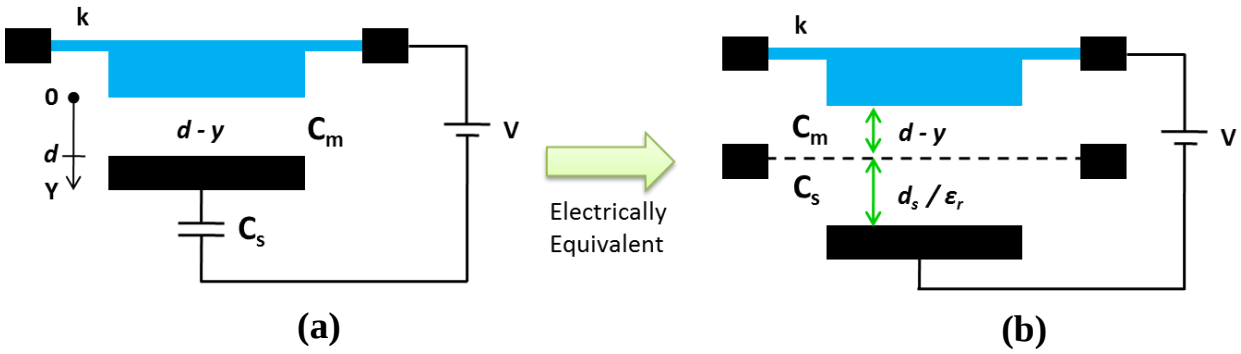


Figure 1.3: Elimination of pull-in effect, reproduced from [5]. (a) Fixed capacitor, *Cs*, is added in series with the mechanical capacitor, *Cm*. (b) Electrically equivalent schematic of structure showing effective gap for actuator.

There are other techniques that can be used to manipulate the pull-in condition of electrostatic actuators. One such method uses charge control rather than voltage control [5]. However, charge control can be difficult to implement using a charge pump and parasitic

capacitances can further alter the ability to control the moveable electrode's position. For the purposes of this work devices will be found solely within the pull-in regime. The term "operation voltage" will be used interchangeably with the pull-in voltage.

1.3.2.2 Switching Speed

The operation speed of a nano-mechanical switch is limited by the time it takes for the moveable element to travel the distance of the air gap. Whereas MOSFETs are limited by RC time constants, NEMS are restricted by their mechanical delay. Starting with the equation of motion for a spring – mass system with electrostatic drive, the closed – form solution for the switching time of a simple beam or cantilever can be found assuming the system is inertia limited. An inertia limited system can be described as a beam with a small damping coefficient (minimal air damping, etc.) and a substantial quality factor, $Q > 2$ (minimal dissipation in beam anchors and internal losses) [7]. The equation of motion is given by:

$$m\frac{d^2x}{dt^2} + kx = -\frac{1}{2}\frac{\varepsilon_o A V^2}{d^2} \tag{1.12}$$

with m being the mass of the mechanical element, and d being the initial gap size of the device. No term for damping appears due to the assumption of small damping coefficient, $b \approx 0$. The external force (driving force) is represented by the electrostatic force, which is assumed to be constant and equal to the initial applied force before actuation. The solution for transit time of the beam determined by Equation 1.12 is given by [7, p. 68]:

$$t_s \cong \sqrt{\frac{27}{2}}\frac{V_{PI}}{V_S \omega_o} \tag{1.13}$$

with V_S being the supplied voltage and ω_o being the resonant frequency of the device. Therefore, a larger applied voltage (in excess of the pull-in voltage) results in a decreased switching time. However, depending on the application, it may be favorable to use voltages closer to V_{PI} to eliminate the need for excessive charging of dielectrics. Additionally, the switching time is inversely proportional to the resonant frequency of the beam/cantilever. A stiffer beam, with higher *k*, results in a lower switching time for a given pull-in voltage. On the other hand, a larger *k* results in a higher pull-in voltage, in accordance with Equation 1.9. The gap size can be independently reduced to bring down the pull-in voltage. Therefore, a tradeoff generally exists between pull-in voltage and switching time [8]. By switching to a material system such as carbon nanotubes, mass density can be substantially reduced to increase the switching speed, while pull-in voltage can still be maintained at low voltages [9]. Another way to further decrease the switching time is to pre-bias the beam (at a voltage less than V_{PI}) so that it is partially deflected at the time the full voltage is applied for turn-on [10]. The switching times evaluated from Equation 1.13 assume that the cantilever/beam do not bounce upon impact/contact.

The turn-off time for the switch is determined by the amount of time it takes for the moveable electrode to lose electrical contact with the fixed contact. Therefore, a small gap of a few nanometers is sufficient to eliminate any tunneling current. Although this represents a short turn-off time, the true turn-off time (i.e. time before returning to initial position) will depend on the *Q* of the mechanical system. A device with large *Q* will oscillate until its energy is dissipated at which point it comes to rest.

1.3.2.3 Reliability and Contact Resistance

The reliability of contact nanomechanical switches mainly depends on the long term stability of the electrical contacts. Contact failure usually occurs as a result of permanent adhesion at the contact interface or contact resistance degradation during repeated cycling of the switch. Adhesion at the contact interface can be the result of microwelding or surface adhesive forces such as van der Waals [11]. Contact resistance degradation can be the outcome of numerous impacts between surfaces and plastic deformation of contacting surfaces [12]. In order to understand the various mechanisms responsible for device failure, a deeper understanding of nanoscale mechanical contacts must be put forth.

The initial premise for modeling nanoscale physical contacts is that contact surfaces always have some degree of roughness, and consequently all contacts are made at local asperities [11][13]. Figure 1.4 illustrates a number of typical scenarios that occur with NEMS contact switches. The first scenario occurs when the impact velocity of the moveable element is relatively low, thereby producing primarily elastic deformation. A switch operating in this regime would exhibit highly reproducible electrical behavior, assuming the absence of surface contamination and oxidation. Alternatively, a fast switch may cause plastic deformation of material upon impact, as seen in Figure 1.4(b). This scenario causes defects in the metallization of contacting surfaces and variations in the resistance of the switch of repeated cycles. Depending on the roughness of the material, only a single point of contact may be achieved. As impacts continue to occur, the cross-sectional area of the contacting surface will evolve and tend towards larger areas of physical contact. Figure 1.4(c) demonstrates another potential scenario for nanoscale contacts. A small change in local surface roughness can result in a substantial

variation in the number of points of contact between the electrodes. Therefore, contact resistance can vary significantly from device to device and during device operation [14].

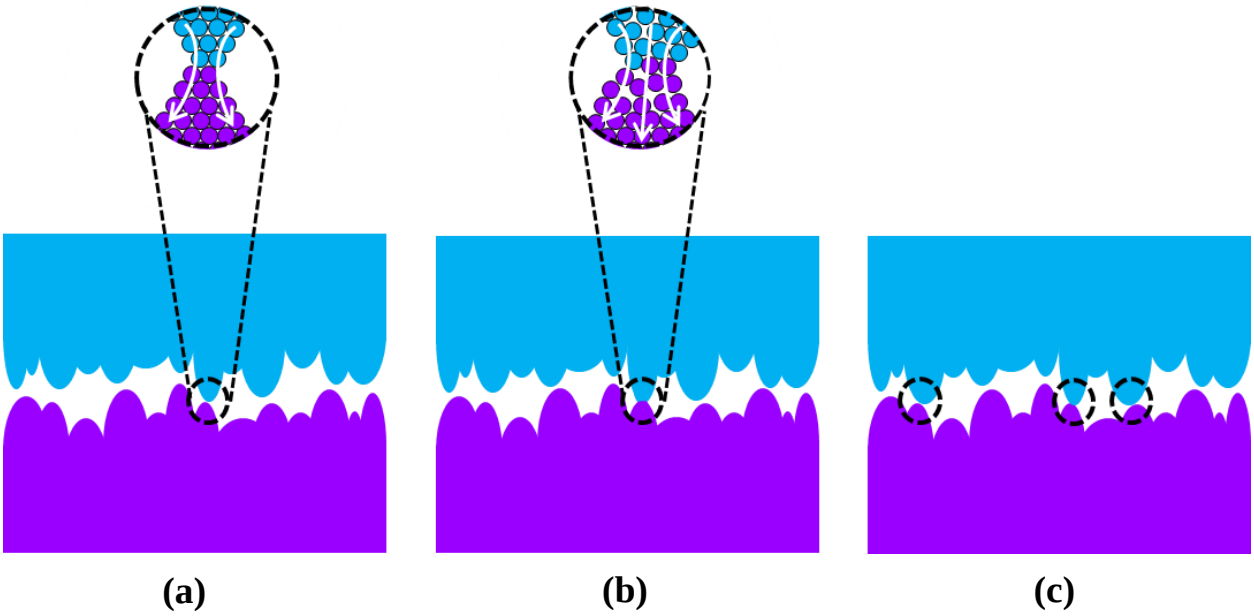


Figure 1.4: Schematic illustrating physical contact of nanoscale surfaces. (a) Contact occurs between single metal grains. For a low impact velocity, elastic deformation is possible. (b) Larger impact velocity causes plastic deformation of metallic electrodes, defects in crystal structure, and potentially increases cross-sectional area of contact. (c) A similar contact can result in a different number of physical channels for conduction.

Although the electrodes themselves have a given resistance, dependent on the particular material's properties and attributes as deposited, the primary contribution to the switch resistance comes from the contact resistance between the nanoscale surfaces of the electrodes. If the radius of the contact area is on the order of the electron mean free path, λ, for the particular electrode material, then both lattice scattering and boundary scattering contribute to the contact resistance. For a circular contact of radius a, the contact resistance, R_c, has been accurately expressed by the following equation [15][16]:

$$R_c = \gamma\left(\frac{\lambda}{a}\right)R_M + R_S \tag{1.14}$$

$$R_c = \frac{1 + 0.83\left(\frac{\lambda}{a}\right)}{1 + 1.33\left(\frac{\lambda}{a}\right)}\frac{\rho}{2a} + \frac{4\rho\lambda}{3\pi a^2} \tag{1.15}$$

Where R_M is the Maxwell spreading resistance due to lattice scattering, R_S is the Sharvin resistance due to boundary scattering for small constrictions, $\gamma\frac{\lambda}{a}$ is a scaling function that accounts for the size dependent contribution of the Maxwell resistance to the contact resistance, and ρ is the electrical resistivity [15][17]. For instance, the mean free path of gold is about 38 nm [18], which is comparable to the grain size seen in electron beam evaporated gold thin films, with grain approximately equal to the film thickness [19]. Furthermore, the effective radius (r) of an elastically deformed contact spot is related to the electrostatic force that makes contact (F_e), the end radius of curvature of the asperity (R_t), and Young's Modulus (E), as follows [20] [21]:

$$r = \left(\frac{3F_eR_t}{4E}\right)^{1/3} \tag{1.16}$$

And for a pressure on the contact that exceeds approximately $0.6H$, where H is the hardness of the material, the material undergoes plastic deformation, and contact radius is described by a different relationship [21]. Therefore, for soft metals, such as gold, low contact resistance is more easily attained, with MEMS devices showing resistances of less than 1Ω [7]. However, Joule heating from current flow can cause micro-welding and even diffusion of atoms across the contacts, which can ultimately lead to device failure [22]. This is particularly problematic for "hot switching" when an applied voltage appears across the contact at the time physical contact is made. Therefore, high melting temperature metals, such as Tungsten, can serve as a potential solution depending on the requirements for resistance. Furthermore, metals with native oxides can inhibit current flow and are generally not beneficial materials for contact switches. The

effect of surface adhesive forces on contact switches has recently been given more attention. Preliminary results suggest that surface treatment with deposition of materials having low Hamaker constant (i.e. ~ 0.5 nm TiO_2) can reduce the effect of van der Waals forces [11]. Although MEMS contact switches have demonstrated billions of cycles with an on resistance of 1.5 Ω [23], NEMS contact switches have shown only 100's to 1000's of cycles with high on resistances for devices that repeatedly switched (~MΩ) [24]. Further materials and device research will be required to determine whether highly reproducible switching with low contact resistance will be possible at the nanoscale.

1.3.3 Varieties of Nanoscale Switches

Nanomechanical switches come in primarily three varieties (Figure 1.5): two-terminals (2T), three-terminals (3T), and four-terminals (4T). 2- and 3-terminals devices can be rather simple to fabricate, requiring only one lithographic mask for devices based on in-plane motion. 4-terminal devices generally involve increased complexity; however, utility also vastly increases making implementation more practical. The following sections will discuss the advantages and disadvantages of each design, while focusing on the aspects of nanomechanical switches that lead to practical devices. Distinctions between designs will be made based primarily on two criteria: ability to isolate the pull-in voltage from the switch conduction path, and independence of the pull-in voltage from the Source/Drain voltages. These two criteria are useful for determining nanorelay reliability and compatibility with circuit implementation, respectively.

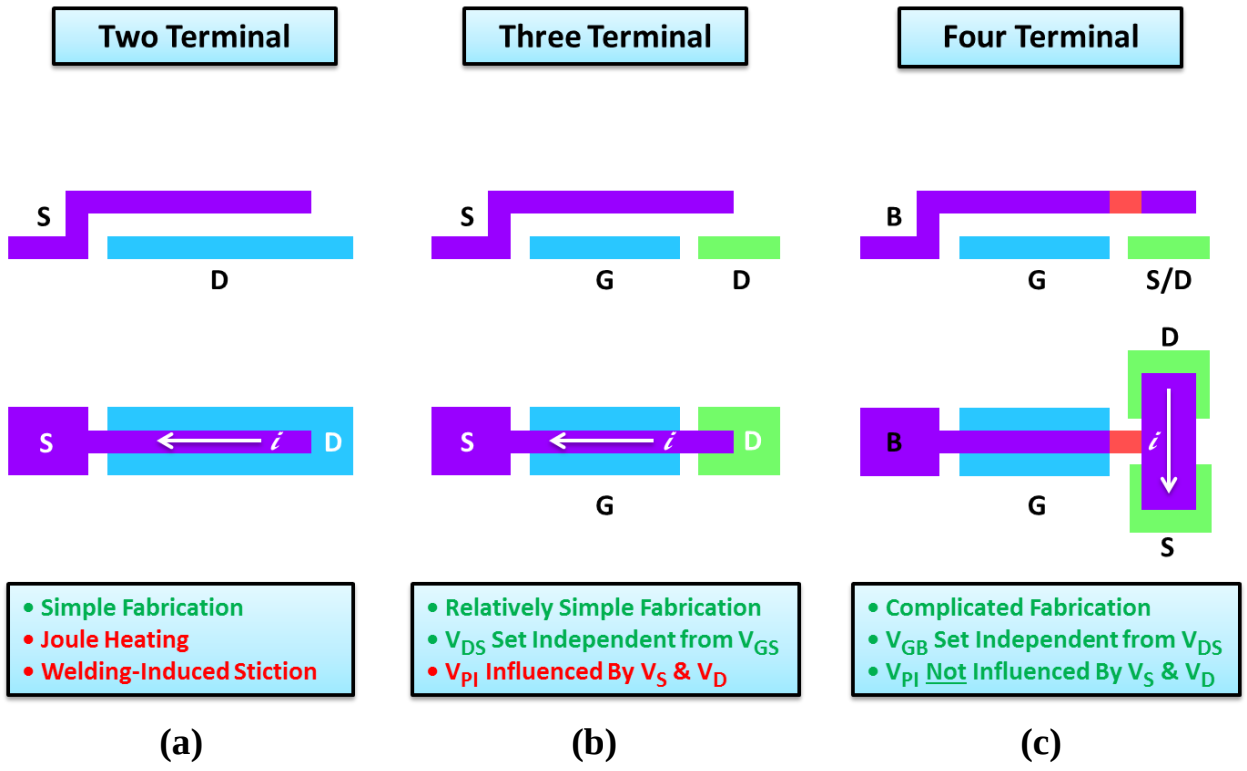


Figure 1.5: Summary of nanomechanical switch architectures. (a) 2-terminal device with only Source and Drain electrodes. (b) 3-terminal device with Source, Drain, and Gate electrodes. (c) 4-terminal device with Source, Drain, Gate, and Body electrodes.

1.3.3.1 Two Terminal

The operation of a two terminal device, as shown in Figure 1.5(a), has been discussed earlier in Chapter 1. The Source and Drain electrodes used for applying the pull-in voltage also serve as the conduction channel after contact is achieved, as seen in Figure 1.6(b). Considering NEMS switches tend to operate from a few volts [25] to a few tens of volts, and single (or few) nanoscale points of contact are expected, as discussed in Section 1.3.2.3, large current densities for low resistance devices can cause burn-out or micro-welding of two-terminal structures. Joule heating is particularly detrimental in 2T structures. As a result of these shortcomings, 2T structures are not particularly useful for circuit implementations.

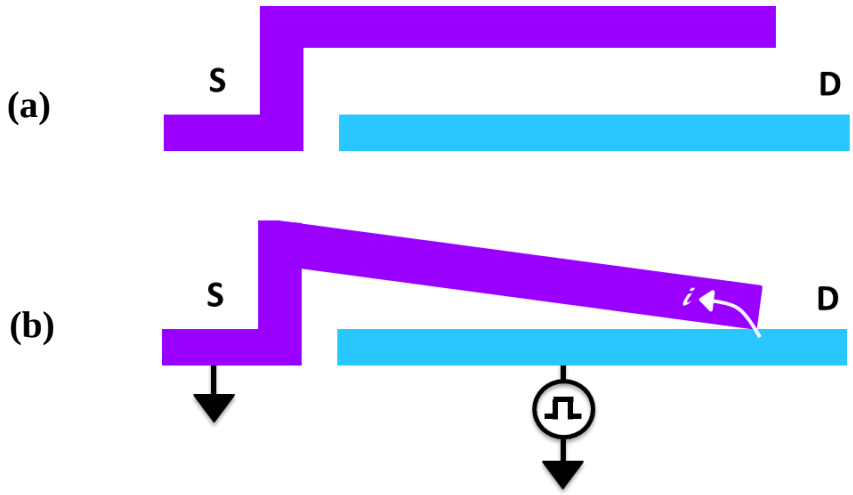


Figure 1.6: A 2-terminal device. (a) Device before actuation. (b) Device after applying $V_{DS} > V_{PI}$. Pull-in results in substantial current flow upon contact.

On the other hand, 2-terminal structures are frequently used for material characterization. The Source and Drain can be the same or different materials. And the structure can be implemented such that the moveable electrode deflects either in-plane or out-of-plane. Additionally, a small area vertical structure can be fabricated using vertically aligned nanotubes or nanopillars, forming a nano-tweezer type structure [26]. The most common uses of 2-terminal structures are for ultrasensitive mass and force detection, and for extracting Young's modulus from electrical or optical based frequency measurements [27]. Recently a novel two terminal non-volatile switch was suggested with one terminal p-type silicon and the other n-type silicon. The device uses surface adhesion forces in combination with the attractive electrostatic force resulting from a diode's built-in electric field to create a memory element [28]. Although two-terminal switches continue to be researched, true switching behavior akin to MOSFET operation (with separate input control for the actuation voltage) is not possible without transitioning to at least 3-terminals.

1.3.3.2 Three Terminal

The principle of operation of the three terminal device is very similar to that of the two terminal device. The main distinction is the added Gate (*G*) terminal seen between the Source and Drain terminals in Figure 1.7(a). The Gate terminal enables actuation via pull-in without the high voltage being seen across the point of contact. The overlap area between the Source and Drain in Figure 1.7(a) is small. Therefore, the Drain has weak capacitive coupling to the Source, and the potential on the Drain has a minimal effect on the pull-in voltage of the device. However, the Source and Gate form the primary parallel plate configuration for determination of pull-in voltage. The voltage difference, $V_G - V_S$, must be greater than the pull-in voltage for proper operation. Hence, a larger Source voltage requires a correspondingly large Gate voltage, as seen in Figure 1.7(b). Meanwhile, the Drain – Source current (I_{DS}) is determined independently of the Gate voltage, and low sensing currents can be used to enable reproducible switching.

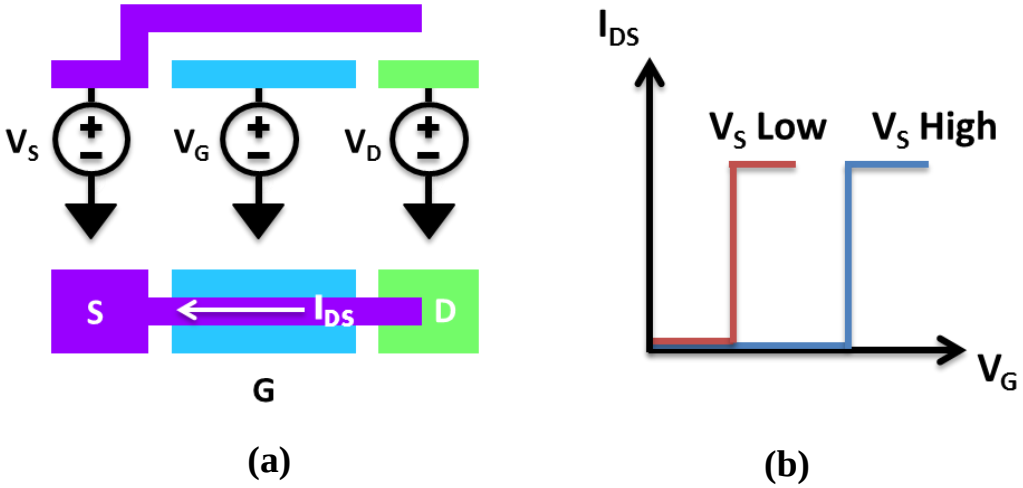


Figure 1.7: Three terminal device operation. (a) Independent biasing of three terminal device. (b) Output characteristics of three terminal device for different Source voltages.

The Source voltage dependent switching behavior outlined in Figure 1.7 leads to further difficulty when the three terminal device is considered for potential applications. For instance, if the three terminal device is used to connect different circuit elements or blocks, such as inverters, then the output of the element connected to the Source would determine the Source voltage. Consequently, the pull-in voltage will fluctuate in accordance with the potential of the Source. One simple solution, seen in Figure 1.8, is to add a programming transistor on the Source side. This enables the Source potential to be pinned during programming of the three terminal switch. Assuming the switch is volatile, the Gate voltage must remain on the device at all times. Therefore, after turning off the programming transistor, the Gate – Source voltage must remain greater than the pull-out voltage, V_{PO}, for all values of the Source voltage to prevent premature pull-out during signal transmission [29]. In summary, the three terminal device solves many of the challenges inherent to the two terminal device, but for most practical applications an additional transistor is necessary, thereby partially diminishing the benefits of mechanical switching. The four terminal device addresses the shortcomings of the three terminal structure.

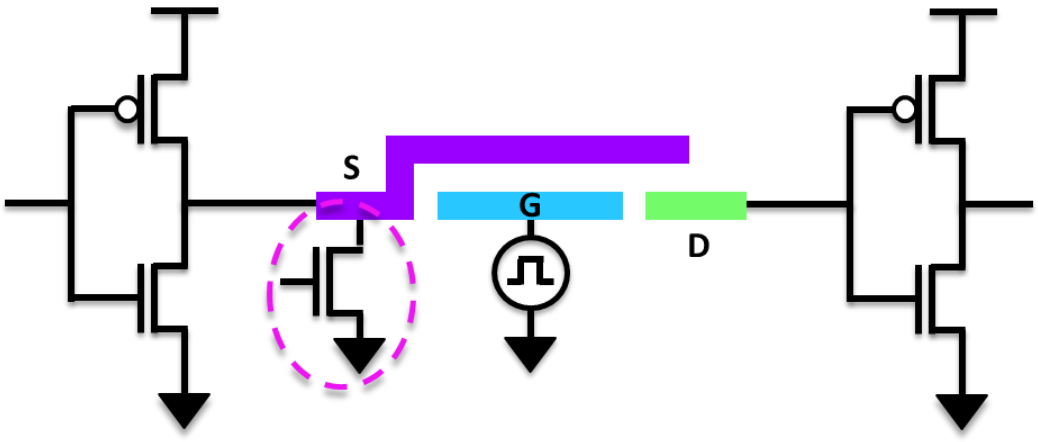


Figure 1.8: Example of difficulty with three terminal device implementation. Programming transistor within dashed oval is necessary to enable consistent operation voltage for three terminal designs.

1.3.3.3 Four Terminal

The four terminal device, as shown in Figure 1.5, adds another terminal, the Body electrode, to further improve the functionality of the switch. The Gate – Body potential difference, V_{GB}, fully controls the switching behavior of the device, independent of the Source and Drain voltages. A conducting channel, used to form the connection between the Source and Drain, is attached to the moveable element (cantilever, etc.), and electrically isolated from the Body electrode by means of an insulating layer or spacer. The Source and Drain overlap with the conducting channel can be very small in comparison to the area of the Gate – Body capacitor, thereby further diminishing the influence of the Source and Drain on the switching behavior. Additionally, metals and other materials used for the conducting channel can be independently chosen and optimized without affecting the mechanical properties of the moveable elements. The four terminal structure provides a practical platform for typical switch implementations based on current CMOS circuit design, making it the most attractive choice for mechanical switches.

1.4 APPLICATION SPECIFIC CONSIDERATIONS

After having described some of the attributes of nanomechanical switches, further attention will be given to the potential applications for this class of devices. The operation voltage, switching speed, and reliability of NEMS switches were addressed in Section 1.3.2. These characteristics will now be discussed in the context of practical applications. Furthermore, consideration will be given to various integration methodologies for future incorporation of nanomechanical switches with existing technologies.

1.4.1 Utilizing Strengths of NEMS

The strengths of NEMS devices are found in their small size and scalability, potential for low voltage operation, minimal energy consumption during switching, significant ON/OFF ratios, suppressed leakage current in off-state, and ease of fabrication. Other properties that have been mentioned in regard to NEMS include radiation and temperature insensitivity [30] [31]. As mentioned previously, the size is only limited by the minimum air gap achievable before onset of tunneling current, ~ 2 – 3 nm. For smaller gaps, NEMS will cease having their near ideal leakage current suppression in the off-state. However, the on-state and associated switching behavior also set a fundamental limit on size scaling. Reproducible switching will become more challenging at small scales. In order for the switch to turn-off (i.e. pull-out) with zero applied voltage, the mechanical restoring force must be greater than the surface adhesive forces [32]. Additionally, a larger mechanical restoring force requires a higher voltage (or larger capacitance) to generate the electrostatic force necessary for pull-in. In summary, the condition for reproducible switching is [11]:

$$k_{min} > \frac{F_a}{d_M} \tag{1.17}$$

where k_{min} is the minimum required mechanical spring constant of the moveable element (for repeated switching), F_a is the surface adhesive force, and d_M is the maximum displacement of the moveable element, as seen in Figure 1.9. The general relationship between k and V_{PI} was shown in Equation 1.9. Therefore, the minimum switching energy for a nano-relay is determined by the energy needed to charge up the parallel plate capacitor (used for electrostatic actuation, C_m) to the pull-in voltage [11]:

$$E_{min} > C_m V_{PI}^2 = \frac{A\varepsilon_r\varepsilon_o}{d_E}\frac{8k_{min}d^3}{27A\varepsilon_r\varepsilon_o} \tag{1.18}$$

$$E_{min} > \frac{8F_a d^3}{27(d - d_M)d_M} \tag{1.19}$$

where d_E is the minimum distance between the capacitive plates, and d is the initial distance between the capacitive plates. Consequently, $d = d_M + d_E$. The offset between the Source/Drain and Gate is necessary to keep the Gate voltage isolated during switching. This offset is accomplished by recessing the gate, as in Figure 1.9, or by using contact dimples [11]. Predictions for minimum energy of aggressively scaled NEMS have ranged from a few aJ [33] to sub-100 aJ [34]. Although van der Waals forces set one limit for minimum switching energy, the switch must also have chemical bonds to form conduction channels for the switch. Therefore, depending on the desired resistance, a certain number of metal to metal bonds will be required. If each bond is ~ 0.2 aJ [35] and 5 bonds are required, then the bond strength of a single contact is ~ 1 aJ. The contribution of van der Waals is approximately another 1 aJ for a 50 x 50 nm^2 contact area [33], making a total minimum energy of 2 aJ for a single contact, and twice that for 4-terminal device (Source and Drain contacts). This doesn't account for the charging of additional parasitic capacitances and fixed capacitors, such as the cantilever anchors, etc. The final conclusion is that active energy dissipation should be on par with scaled MOSFETs, however, the off-state power consumption is vastly improved by virtue of the insulating air gaps. Researchers suggesting the usage of NEMS for logic applications attempt to utilize NEMS switches with multiple inputs/outputs to perform complex logic functions with a single device [32] thereby decreasing the total delay. Using this approach, recent work has shown that ~ 10 times energy savings (depending on fixed capacitance) can be achieved by nanorelays as compared to an equivalent MOSFET technology up to ~ 100 MHz. However, nanomechanical

devices will still be limited in their ultimate speed when compared to solid-state devices for logic.

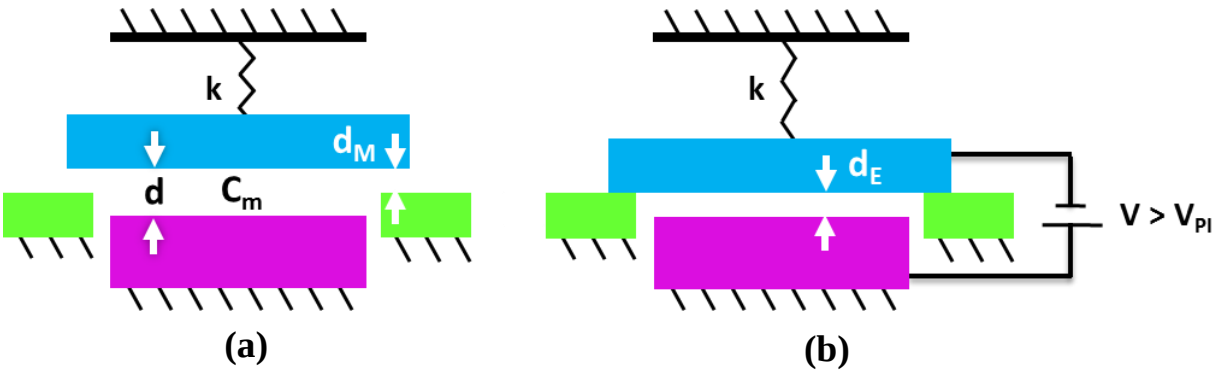


Figure 1.9: Schematic of device for determining minimum switching energy. Device shown here appears to be 4-terminals, but operates like 3-terminal device because Source and Drain voltages are related to electric potential of moveable electrode upon contact. (a) Device before pull-in. Smaller gap, d_M, assures that moveable electrode makes physical contact only with Source/Drain. (b) The gap size, d_E, corresponds to the minimal distance between the capacitive plates after pull-in.

The other main concern when discussing potential applications for NEMS switches is the on-state resistance and reliability, which are interdependent. Whereas repeatable switching with low on-state resistance, on the order of Ω's, has been demonstrated at the microscale [36], nanoscale devices have exhibited a tradeoff between these two properties. Harder refractory metals, although demonstrating exceptional wear and heat resistance, result in slightly higher resistance values [7, p. 200] than many noble metals and have a propensity for oxidation, thereby making contact resistance unstable. The noble metals, such as gold, form low resistance conduction channels even in nanoscale devices [37] but they are also susceptible to microwelding. Therefore, NEMS have not yet proven to be a viable solution for applications that require very low resistance and frequent switching. However, a more interesting suggestion based on current NEMS characteristics is power gating. Power gating is used to shut off

individual functional units of the microprocessor while not in use. Coarse grain power gating is used to shut off large blocks of CMOS devices. However, since transistors serve as the power gates, the power gates themselves contribute to the leakage. As coarse grain power gating moves towards fine grain power gating, shutting off smaller functional units, the number of power gates increase, and leakage increases. Therefore, NEMS switches have been suggested for fine grain power gating [38]. Additionally, functional units that require frequent usage can be power gated by MOSFETs and less frequent systems can be controlled by NEMS. This solution further tailors the usage of NEMS to applications requiring infrequent switching.

Other potential applications for NEMS switches that have been suggested are FPGAs (Field Programmable Gate Arrays) [29], LUT (Look Up Tables), and volatile/non-volatile memory. Non-volatile memory based applications are beneficial since current memory technologies, such as Flash memory, operate at speeds comparable to MEMS/NEMS devices. However, few non-volatile device architectures have been posed using nanomechanical structures [39][40][41]. NEMS switches have also been suggested for FPGAs and LUTs since higher resistance values and infrequent switching are common to both applications [42][29]. Although theoretically there is some potential benefit of using contact nano-electromechanical switches for computation and logic, current NEMS switches appear to be better suited for applications requiring infrequent switching.

1.4.2 3D Integration

A more recent approach to MEMS integration utilizes emerging methodologies common to 3D integration. 3D integration can enable chips or wafers with standard CMOS processing to be merged with dedicated MEMS/NEMS chips. This assures that CMOS will remain unaffected

by post-CMOS processing. Additionally, MEMS/NEMS can be given a larger process temperature latitude and greater variety in material selection and fabrication technologies. Many different methods exist for combining various device layers contained on different substrates. Some of these include: metal-to-metal bonding, oxide-to-oxide bonding, and polymer-to-polymer bonding. Numerous techniques exist to transfer thin single crystal silicon or other thin films for further device processing atop CMOS, while other techniques are used to transfer completed devices. Vias or interconnects are necessary and common to all stacking approaches, thereby enabling communication between device layers. Vias can be formed using via-first, via-middle, and via-last processes depending on the stage at which vias are incorporated in relation to the device fabrication [43]. Ultimately, the density of interconnects and the alignment of layers will limit the connectivity between device layers. Later on, in Chapter 5, further attention will be given to the 3D integration of NEMS with CMOS. A potential high density integration scheme will be suggested for NEMS along with applications based on interconnect densities approaching or exceeding the density of devices.

1.4.3 Process Integration

Although NEMS electromechanical switches have not yet been adopted for widespread commercialization, MEMS devices (actuators and sensors) have already been absorbed into commercial electronics. A number of different techniques have been used to integrate MEMS devices with CMOS. MEMS and CMOS co-fabrication has been attempted [44], however, post-CMOS monolithic integration has proven to be more feasible and less disruptive of the CMOS process flow (given a number of significant process restrictions for the MEMS). The most common approach is known as MEMS-last, whereby MEMS devices are formed via surface

micromachining after completion of the CMOS back – end – of – line (BEOL) process steps. A successful example of this is the digital light process (DLP) from Texas Instruments [45]. Using a metal structural layer for the mirrors, process temperature was kept sufficiently low for underlying CMOS circuitry. Athough there are numerous challenges, there is keen interest in stacking NEMS devices on top of CMOS. The primary benefits are reduced die size, and improved performance by minimizing interconnect distances, and their corresponding parasitics [44].

The main challenge to MEMS-last is the thermal budget for post-CMOS fabrication. For instance, the 0.25 μm CMOS process has shown a thermal budget limit of 10 hours at 425 ˚C [46]. Metal interconnects suffer the most during high temperature post-CMOS processing, showing increased resistance due to thermal stress and annealing effects [44]. Therefore, the most prominent MEMS/NEMS material, poly-Silicon is immediately eliminated as a result of the thermal budget. Additionally, high temperature silicidation cannot be used to form low resistance contacts between the CMOS interconnects and the semiconducting MEMS device layers. Similarly, amorphous silicon, which can be deposited below 400 ˚C, can be difficult to contact. Alternate structural materials have been suggested that require lower deposition temperatures. Promising germanium-based candidates include poly-cyrstalline germanium [47], and poly-crystalline silicon germanium, which can also be deposited below 450 ˚C [48][49]. Poly-crystalline germanium-based structural materials still enable high quality factors (low damping losses) for resonator applications, high mechanical strength, and low resistance contacts using Aluminum [50]. One additional area that has been given attention is metal-based structural layers. Some examples include gold (Analog devices MEMS series switch), aluminum (Lincoln Lab MEMS series switch) [51], and platinum [52].

Aside from the previously mentioned difficulties, optimization and control of thin film stress is extremely essential for structural layers. Furthermore, the choice of sacrificial layers can be equally challenging. Etching of sacrificial silicon dioxide can cause damage to underlying CMOS passivation layers, such as silicon nitride, etc. Ultimately, many constraints exist for devices fabricated using the MEMS-last process. Therefore, a more CMOS and MEMS friendly process is desirable.

1.5 LITERATURE REVIEW

This section will be used to summarize the previous work pertaining to contact nano-mechanical switches based on electrostatic actuation. Devices will be reviewed and analyzed based on the primary metrics discussed in Section 1.3. Figures of merit generally include operation voltage, switching speed, and reliability. For the purposes of this work, greater focus will be put on device footprint size, simplicity of fabrication (ease of scaling), and the utility of the design (number of terminals). Material considerations as well as practical process challenges will be discussed. Furthermore, a systematic method of device categorization will be used to illustrate the novelty of the device demonstrated here-in.

Fabrication can generally be categorized as either a top-down or bottom-up approach. A top-down approach starts with bulk or thin film material, either grown or deposited, and ends with micro- and nano-patterned structures. Mechanical and chemical methods are used to define and etch the material to produce the desired nano-structure. Bottom-up fabrication uses chemical means to form nano-structures from smaller molecular or atomic building blocks. Chemical vapor growth using a catalyst particle enables growth of nano-tubes and nano-wires in pre-defined locations. Also, self-assembly is used to form nano-scale organized structures starting

from a disorganized system. Although MEMS devices have been fabricated solely using top-down process techniques adopted from standard CMOS fabrication, aggressively scaled NEMS devices have incorporated both top-down and bottom-up approaches. Silicon nanowires and carbon nanotubes/fibers have been used to create novel electro-mechanical switches. Furthermore, bottom-up approaches can result in vertically aligned high-aspect ratio nanowires, useful for small area switches. Without the high-aspect ratio features achieved in growth-based approaches, top-down approaches remain planar, where the aspect ratio of the mechanical element can be defined by thin film processes or lithography and etching. The following sections will be used to examine specific devices fabricated using top-down and bottom-up approaches, as well as planar and vertical structures.

1.5.1 Top-Down Planar Approach

The most common MEMS and NEMS structure is the top-down planar device. Standard deposition and etching processes are used to micro-machine planar cantilevers and beams. Actuation of the moveable element can be categorized as in-plane (lateral), out-of-plane, and torsional motion. Displacement can also be attributed to a combination of these mechanisms. The top-down planar approach is characterized by its ease of fabrication, tight control of device placement and critical dimensions, and assembly using standard processing techniques.

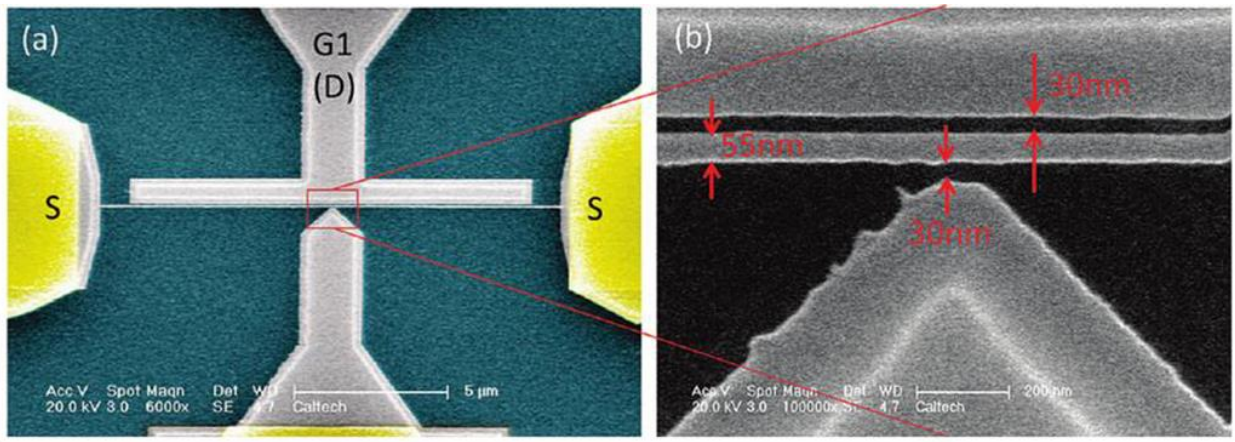
1.5.1.1 Lateral Design

Lateral top-down planar devices use in-plane motion of a moveable element to form a switch with generally three independent terminals. All electrodes and mechanical elements are planar, with the geometry defined and patterned using typically a single step of lithography.

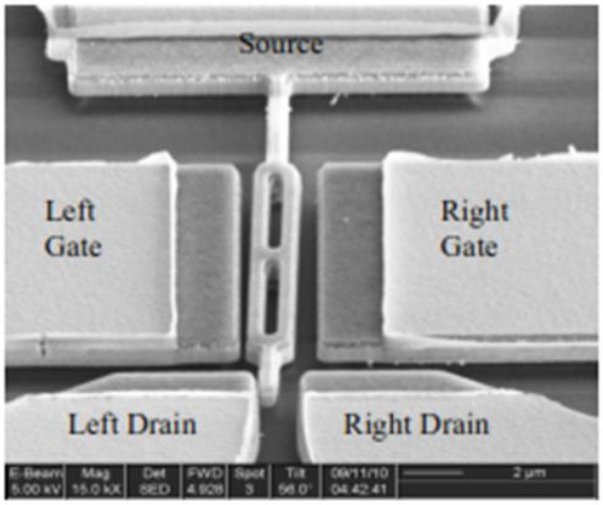
Figure 1.10 displays a few devices representative of the general approach taken in lateral top-down structures. The structural layer usually consists of a thin film that is grown or deposited on a sacrificial layer (typically silicon dioxide). Electron beam or optical lithography is used to define the critical dimensions, namely the beam/cantilever width and the nanoscale air gaps. The pattern is transferred into the mechanical layer using highly anisotropic etching. Vertical sidewalls are necessary, as they define the point of contact and effective size of the air gap. Isotropic etching is used to release the mechanical structure.

Figure 1.10 (a) shows a doubly-clamped beam composed of SiC deposited using atmospheric pressure chemical vapor deposition. SiC thickness is ~ 45 – 50 nm. Beam dimensions as pictured are length of 15 μm, width of 55 nm, and air gap of 30 nm. Operation voltage of the device is ~ 7.8 V [8]. A two-terminal device is displayed, with aluminum metallization of the pads. Switch on-resistance is on the order of tens to hundreds of kΩ's. Figure 1.10 (b) shows a typical three-terminal planar device. The Gate electrode is recessed from the Source and Drain electrodes. The mechanical layer consists of 1 μm of poly-silicon on top of 2 microns of silicon dioxide. A clamped – free beam was fabricated with length of ~ 20 μm (5 μm with narrow width, 15 μm with increased width), approximate width of 0.5 μm, and air gap ~ 0.5 μm. Operation voltage of the device is ~ 14 V, with platinum metallization on pads on contact points [53]. Both of the previous two examples are fairly large, micron scale. A slightly smaller version of a three-terminal device with cantilever lengths of 2 – 4 μm's using poly-silicon on silicon dioxide is shown in Figure 1.10 (c). The cantilever thickness is ~ 173 nm and the gap size is ~ 66 nm. The version with a 4 μm long cantilever has an operation voltage of ~ 10 V [54]. All of the aforementioned devices are relatively easy to fabricate, however, since

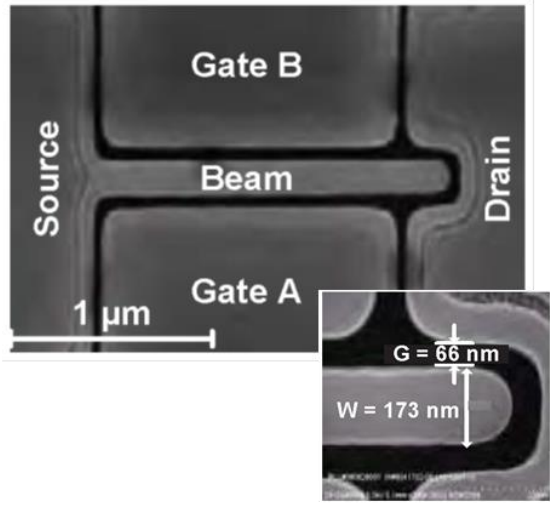
all the critical dimensions are lithographically defined, advanced lithography and etching techniques are required to further scale size and operation voltage.



(a) X. L. Fang et al., Caltech, 2010.



(b) R. Parsa et al., Stanford, 2011.



(c) H. F. Dadgour et al., UCSB, 2010.

Figure 1.10: Examples of top-town lateral device structures. (a) Work performed at Caltech using patterned SiC thin film for form doubly-clamped beam. Two-terminal devices pictured with Source and G1 (Drain) terminals. (b) Work performed at Stanford using patterned poly-silicon thin film on silicon dioxide. Multi-terminal device pictured. Operation is akin to three-terminal device with Source, Drain, and Gate. (c) Work performed at UCSB using patterned silicon on silicon dioxide. Scaled device shown with cantilever length of ~ 2 µm.

1.5.1.2 Out-of-Plane Design

Out – of – plane top-down planar structures use multiple thin film layers to build up a structure designed for out – of – plane motion. The size of the structure is lithography defined, however, all critical dimensions (cantilever/beam thickness and air gap size) are defined by thin film processes. Complicated structures can be fabricated using this approach with number of terminals ranging from 2 – 4 (with more than 4 terminals possible for increased functionality).

Top-down out-of-plane structures generally start with the patterning of electrodes on top of an insulating layer. Next, a sacrificial layer is deposited on top of the electrodes. Then the structural layer is deposited and patterned. And finally the structure is released using an isotropic process. Figure 1.11 summarizes the general thrust of work being done using a top-down out-of-plane approach. Figure 1.11 (a) shows a simple two-terminal device that is aggressively scaled. A TiN singly clamped cantilever of length 300 nm, thickness 35 nm, and air gap 15 nm exhibits an operation voltage of ~ 13 V [24]. A similar device, with three-terminals is shown in Figure 1.11 (b). 2 to 3 lithographic steps can be used to fabricate such a device. The switch consists of a singly clamped gold cantilever of length 1050 nm, thickness 50 nm, and air gap 100 nm. Operation voltages range from 4 V to 22 V, with on-resistance values of hundreds of Ω's to tens of Ω's, respectively. Switching times are calculated to be ~ 55 ns [37].

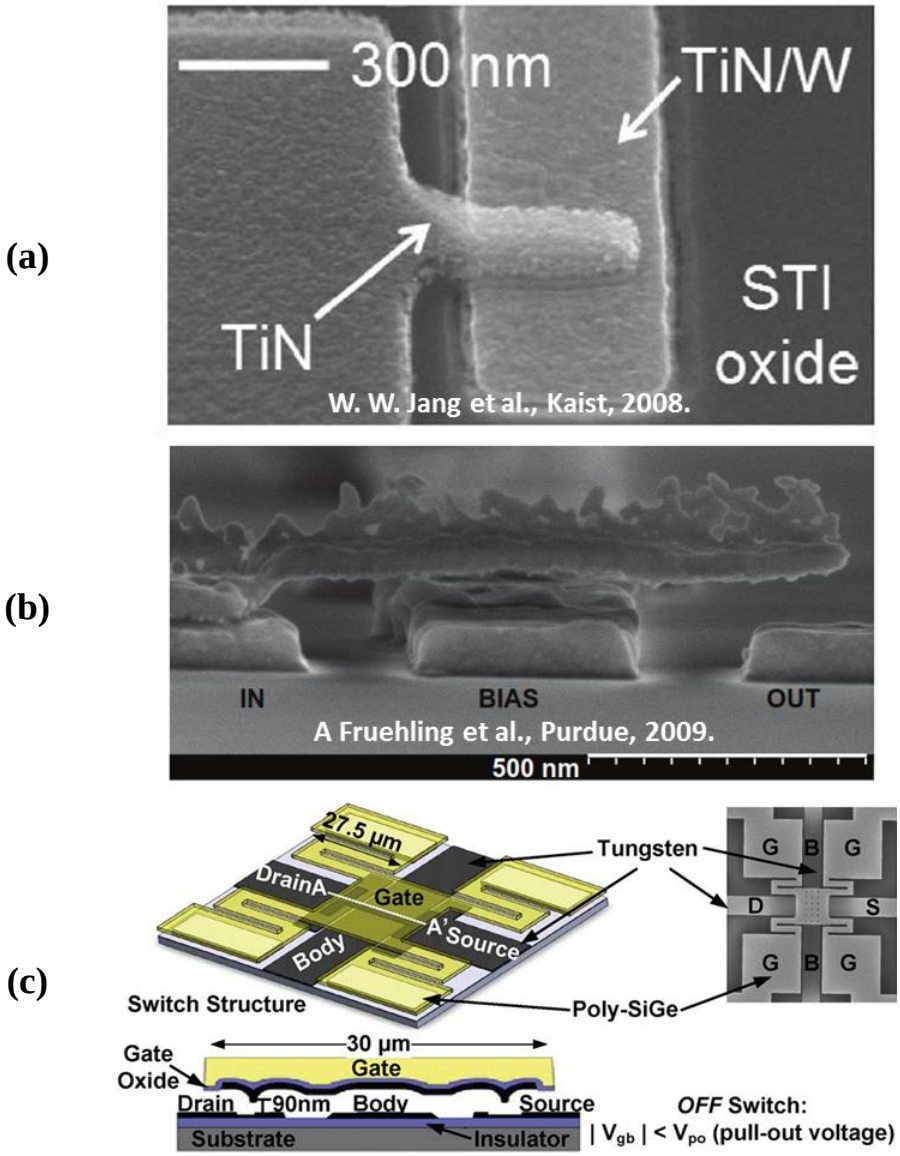


Figure 1.11: Examples of top-down out-of-plane devices. (a) A two-terminal device with 35 nm thick TiN singly clamped cantilever and 15 nm air gap. (b) A three-terminal device with 50 nm thick Au singly clamped cantilever and 100 nm air gap. (c) A four-terminal device with increased complexity consisting of a poly-SiGe movable structure by folded flexures.

One other work of interest which has been thoroughly investigated is a four-terminal switch which is still on the micro-scale, but currently poised for further scaling. Figure 1.11 (c) shows a device that uses a poly-SiGe Gate structure supported by folded flexures to cause a thin

tungsten layer to form a conduction path between an independent and electrically isolated Source and Drain (isolated from the Gate/Body). Device dimensions are quite large, with fold flexures taking up tens of microns, and the Gate structure also having a width of ~ 30 μm. Air gaps between tungsten dimples and electrodes are ~ 90 nm. Operation voltage is ~ 8 – 10 V with switching time on the order of 10's of μs [55]. Reproducible switching has been exhibited with this micron scale device, and a nanoscale version has been investigated and considered for circuit implementation. A four mask process is used to fabricate the device. All of the previous devices utilize thin film thicknesses to control critical dimensions. Aggressively scaled devices have already been achieved using this approach. Furthermore, out-of-plane structures enable designs of increased complexity and usability, with simultaneous contact of multiple electrodes possible.

1.5.1.3 Torsional Design

A torsional top-down switch has similar fabrication and operation to the out-of-plane top-down switch. The main difference is that torsion is used to cause the deflection of the moveable element. However, the direction of motion is still out-of-plane. This category of devices has seen the least exploration. Figure 1.12 shows a simple two-terminal device that uses an electrostatic force exerted on a cantilever with a thickness of 220 nm, length of 9 μm, and air gap of 80 – 100 nm. Two torsion bars support the cantilever, with length of 2.4 μm and width of 530 nm. The force on the cantilever applies a torque on the torsion bars to cause actuation of the switch. An operation voltage of ~ 5.5 V is observed for these devices. The main advantage to a torsional based device is that electrostatic force can be optimized independently from the mechanical properties. Capacitive area of the cantilever can be maintained while torsion bars can be made less stiff [56].

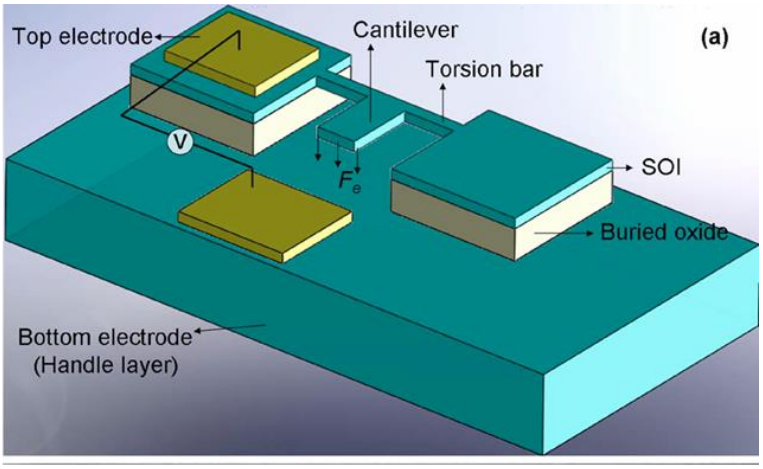
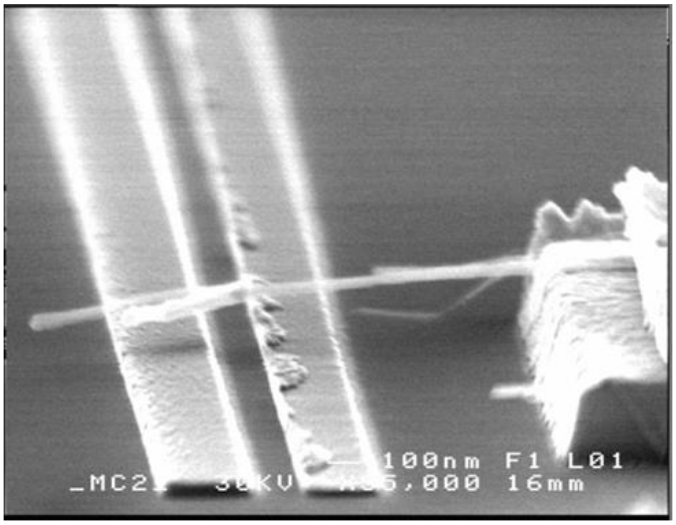


Figure 1.12: Example of top-down torsional device. Two-terminal structure made from SOI.

1.5.2 Bottom-Up Planar Approach

Bottom-up planar devices are an extension of top down planar devices. Geometry stays nearly the same; however, the mechanical element is replaced with a nanowire or nanotube. Controlling the orientation (direction), location, and size of bottom-up self-assembled or grown nano-structures is challenging [57]. Scaling analysis of carbon nanotube based NEMS devices has been explored by analyzing the effect of nanotube diameter distribution on operation voltage for device and circuit applications [58]. Some of the approaches used for making nanotube based devices include: random dispersion and individual placement, growth on optimized substrate and transfer to handle wafer for device assembly, directed self-assembly, and patterned growth using nanoscale catalyst particles [25]. Bottom-up devices tend to have between 2 and 3 terminals. Nanotube and nanowire mechanical structures are of particular interest because they offer extremely high aspect ratios at a very small scale.



S. Axelsson et al., Chalmers Univ. of Tech., Goteberg Univ., Seoul National Univ., 2005.

Figure 1.13: Example of bottom-up planar structure using a carbon nanotube as a mechanical element. Three-terminal device is shown. Device operates using out-of-plane motion.

Figure 1.13 shows an assembled bottom-up nano-relay based on carbon nanotube mechanical element. Plasma enhanced chemical vapor deposition was used to grow multi-wall carbon nanotubes with diameters generally ranging from 20 – 50 nm. Gold electrodes are patterned for the Drain and Gate. Additionally, a raised Source electrode (~ 135 – 200 nm above the Drain/Gate) is used to create a platform for a suspended nanotube. PMMA is spun and etched back to the Source electrode, nanotubes are dispersed and aligned using ac-dielectrophoresis, a top electrode is deposited on the Source side of the nanotube, and PMMA is removed to release the CNT. The length of CNTs was ~ 2 – 3 μm. Operation voltage was demonstrated at ~ 5V [58]. Variation in nanotube diameter and length resulted in varying degrees of success during the release process. Fabrication difficulties are plentiful for bottom-up planar structures.

1.5.3 Bottom-Up Vertical Approach

Building on the previous work, a slightly more robust approach has been investigated using vertically aligned carbon nanotubes. Unlike all the prior work that constructs the mechanical element in a planar configuration; vertical structures truly take advantage of space in three dimensions. Consequently, the length of the mechanical element, which is typically the largest dimension of a nanoscale switch, can be transposed to a vertical orientation, thereby minimizing the area of the device. Low voltage operation with high aspect ratio structures can be achieved in the smallest are possible. Figure 1.14 shows a bottom-up vertical device with three terminals. Two-terminal devices with vertically aligned CNTs have also been demonstrated for switching applications and nano-tweezer type structures [26]. The device in Figure 1.14 was fabricated using nickel catalyst dots (~ 150 nm diameter) on top of niobium electrodes to control the growth of multi-wall CNTs (MWCNT). The height of the nanotubes is ~ 2 μm and the diameter is ~ 70 nm. Operation voltage of the device is ~ 22.5 V [59]. This voltage is not particularly low for such high aspect ratio structures. This may be the result of a high value for Young's modulus of MWCNTs. Reported values are on the order of ~ 1 TPa [60][61]. And pull-in voltage goes as $\sqrt{E}$. And bulk silicon has a Young's modulus of ~ 169 GPa (for a cantilever with axis of bending in the <110> direction) for the sake of comparison [62]. Vertical bottom-up structures introduce an interesting and novel use of space for switching applications. However, growth based approaches still require more future development and unconventional processing than their planar counterparts.

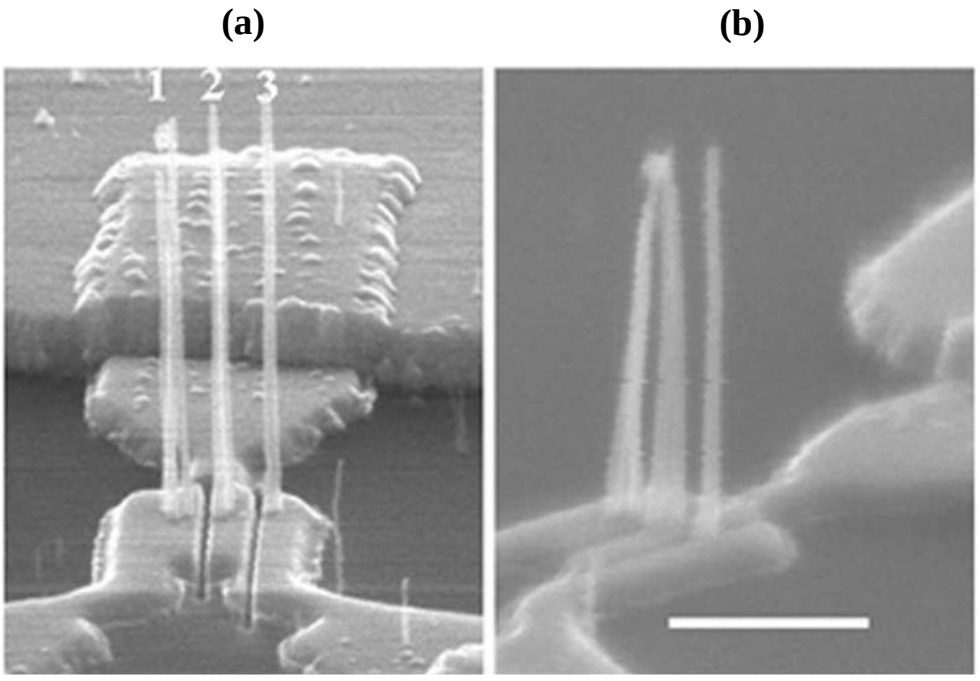


Figure 1.14: Example of bottom-up vertical device using vertically aligned carbon nanotubes. Three-terminal device shown. Pre-patterned catalyst dots use to define growth sites for MWCNTs. Height of nanotubes is ~ 2 μm and diameter is ~ 70 nm. Scale bar is 1 μm.

1.6 NOVELTY OF OUR APPROACH

The ideal contact nanomechanical switch takes up the least amount of real-estate, has relatively simple fabrication, and is useful for circuit and other integrated applications. This thesis will describe such a device. The work herein will demonstrate, for the first time, the possibility of using standard top-down fabrication techniques and a single step of optical lithography to assemble a compact multi-terminal vertical nano-relay.

After having reviewed the current work related to contact nanomechanical switches, the novelty of the work described herein will be clearly identified in light of numerous practical

device considerations. Figure 1.15 shows a summary of the key features needed for useful devices and aggressive scaling. Orientation describes the geometry of the device. Typical number of electrodes describes the likelihood for decoupling the Source/Drain potential from the Gate actuation voltage. Section 1.3.3.2 discussed the influence of the Source or Drain potential on the operation voltage for a three-terminal device. Two-terminal devices have no immunity to the state of the Source and Drain potential. Three-terminal devices provide isolation from the actuation voltage, and partial decoupling from the electrode not connected to the moveable element. Four-terminal devices can theoretically decouple the Source/Drain from the actuation voltage applied across Gate/Body electrodes. Some of the entries in the chart (for number of terminals) have not been demonstrated, however, they should be possible without great difficulty. Devices can have more than four terminals, however, basic operation of a single nano-relay does not greatly change after incorporating a Gate, Body, Source, and Drain (although increased functionality and computing may be possible). Difficulty of fabrication and area describe the scalability and potential for mass production of the particular approach.

Figure 1.15 categorizes the current approaches to nanomechanical device design. Prior to the work contained in this thesis, all top-down fabrication resulted in planar electro-mechanical structures. Vertical structures had only been attempted using bottom-up fabrication. The work herein takes advantage of mature top-down fabrication techniques to construct a vertical switch. Additionally, designs for three and four terminal devices are achievable, with operation similar to planar structures. Since scaling of nanomechanical switches is limited by the stiffness (dimensions) of the mechanical element, a high aspect ratio vertical switch provides the greatest potential for scaling. However, electromechanical devices are highly sensitive to size variation of the mechanical element and air gap size of the variable capacitor. Therefore, bottom-up

growth based approaches suffer due to variation in size and placement, which correspond to mechanical stiffness and air gap size.

Fabrication Method	Orientation	Typical Number of Electrodes	Difficulty of Fabrication	Area
Top Down	Planar (Lateral)	2 – 3	Low	Average
Top Down	Planar (Out-of-Plane)	2 – 4	Moderate – High	Large
Top Down	Planar (Torsional)	2 +	Moderate	Large
Bottom Up	Planar	2 – 3	High	Average
Bottom Up	Vertical	2 – 3	High	Small
Top Down	Vertical	3 – 4	Low – Moderate	Small

Figure 1.15: Summary of nano-relay fabrication methods and device geometries (orientation). Typical number of electrodes describes the likelihood for decoupling the Source/Drain potential from the actuation voltage. Difficulty of fabrication accounts for number of lithographic steps and potential for mass fabrication. Area describes size and scalability. Highlighted row (last row) describes contribution of the work demonstrated in this thesis.

A top-down vertical device eliminates the difficulties intrinsic to growth based approaches, while still retaining the benefit of a vertical design. Multi-terminal vertical designs were made possible as a result of a novel actuation scheme that uses capacitive coupling of a floating conductor to actuate a nanopillar-based switch. A combination of bending and torsion is also used to overcome challenges inherent to compact multi-terminal devices. Furthermore, low voltage compact devices were fabricated using only a single step of optical lithography and self-

aligned processes. Figure 1.16 shows a novel four-terminal top-down vertical silicon nanomechanical switch [63]. The following sections will discuss the fundamental challenges to designing and fabricating a practical top-down vertical switch.

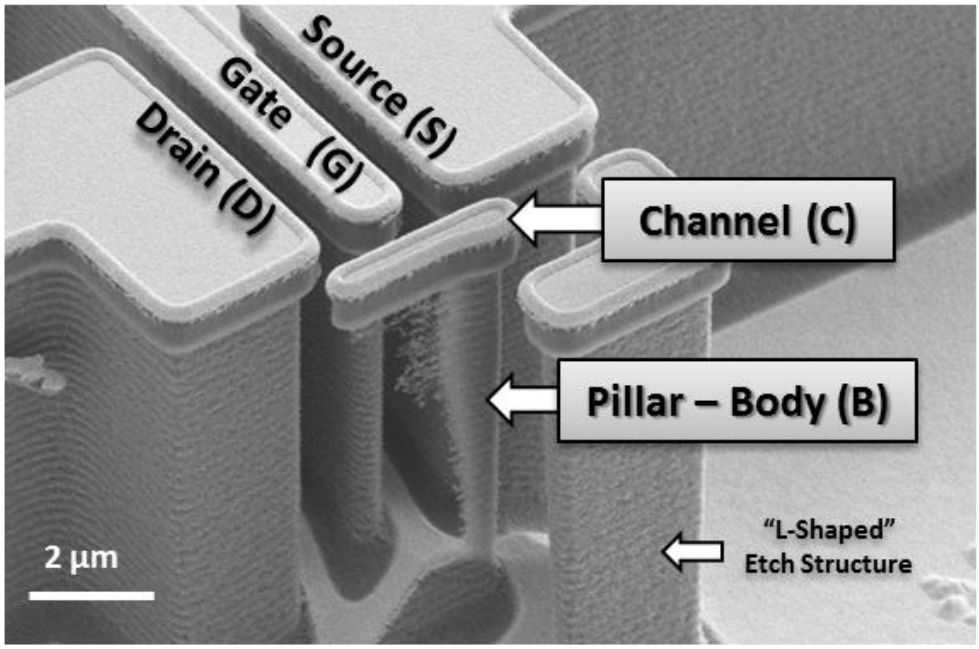


Figure 1.16: SEM image of a top-down vertical silicon nano-electromechanical switch. Four-terminal design. Pillar serves as the Body electrode and is grounded via the substrate during programming. Metallic Channel is electrically floating and serves to connect Source and Drain electrodes.

1.6.1 Electrode Isolation

Although the simplest electromechanical contact switches contain only two terminals, a vertical top-down switch encounters a number of difficulties in a two terminal configuration. By transposing the typical two-terminal structure (i.e. Figure 1.11 (a)) to the vertical direction, an insulating later must be maintained to keep electrical isolation between the fixed electrode and the moveable electrode. This can be accomplished with a silicon-on-insulator (SOI) substrate.

However, contacts must be made to both electrodes in order to generate an electrostatic force, as seen in Figure 1.17 (a). Thin film deposition on the moveable electrode (pillar) can cause unacceptable stress and bending, and increased stiffness. Additionally, electrical isolation between the two electrodes will be extremely difficult.

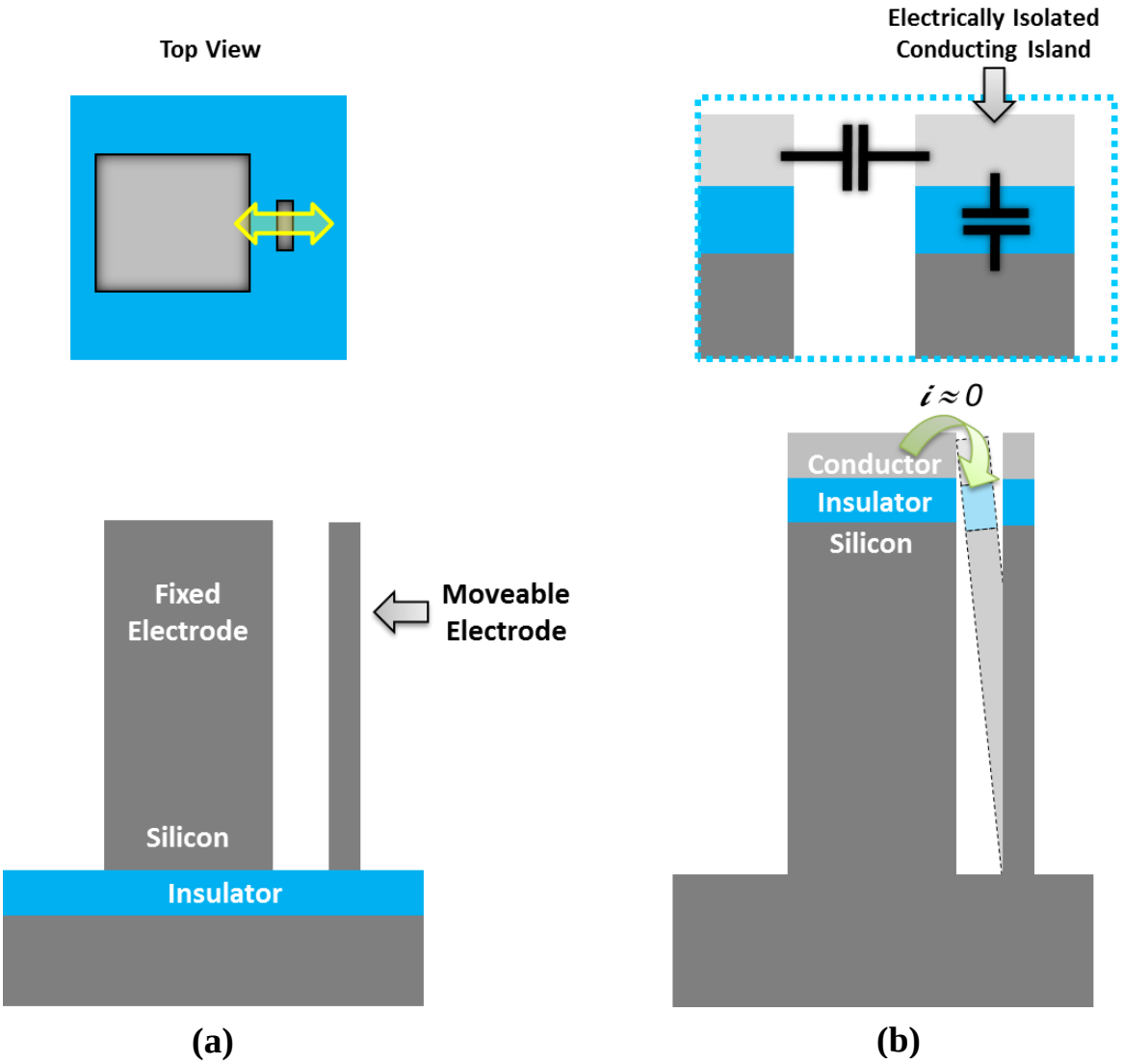


Figure 1.17: Summary of challenges for electrode isolation and device contacts. (a) Top view and side view of two-terminal top-down vertical structure. Structure etched into silicon-on-insulator substrate. Difficulty arises in contacting the moveable electrode. (b) Alternative top-down structure with insulator at top of structure. Removes need for contacting pillar, however, does not serve as a contact switch.

An alternate approach is to move the insulating layer from the bottom of the vertical features to the top, as seen in Figure 1.17 (b). A conducting island must also be formed on top of the insulator. This design creates a capacitve voltage divider that eliminates the need for individual contacts to nanopillars. The substrate can be grounded, and devices can be actuated by applying a bias on the larger fixed electrode. However, this simple two-terminal design does not result in a DC current path upon actuation. The insulating spacer prevents current flow from the fixed electrode to the substrate. Therefore, this approach does not produce a useful contact switch and there is no particularly simple way to create a two-terminal top-down vertical switch. This obstacle leads to the design of a multi-terminal top-down vertical switch.

1.6.2 Multi – Electrode Design

By simply adding an additional terminal to the two-terminal device, a contact electro-mechanical switch can be achieved. Upon actuation of the pillar/island assembly, the island can make simultaneous contact to the Source and Drain electrodes in an ideal device. However, at the nanoscale, small variations in dimensions and surface roughness can lead to local offsets between features. Figure 1.18 (b) depicts a small offset between the Source and Drain electrodes. This offset results in an air gap even after the pillar is actuated. Gaps of a few nanometers are common and easily suppress the on-state current. A nano-ribbon type device with high torsional stiffness prevents correction for small offsets. Therefore, reproducible switching for three-terminal top-down vertical devices is inconsistent and not reproducible. This fundamental problem will affect planar and vertical nanoscale structures that require multiple points of physical contact. Chapters 2 and 4 will present a unique solution that uses torsion and

bending to achieve reproducible switching. A four-terminal device is employed to overcome many of the obstacles common to nanoscale contact switches.

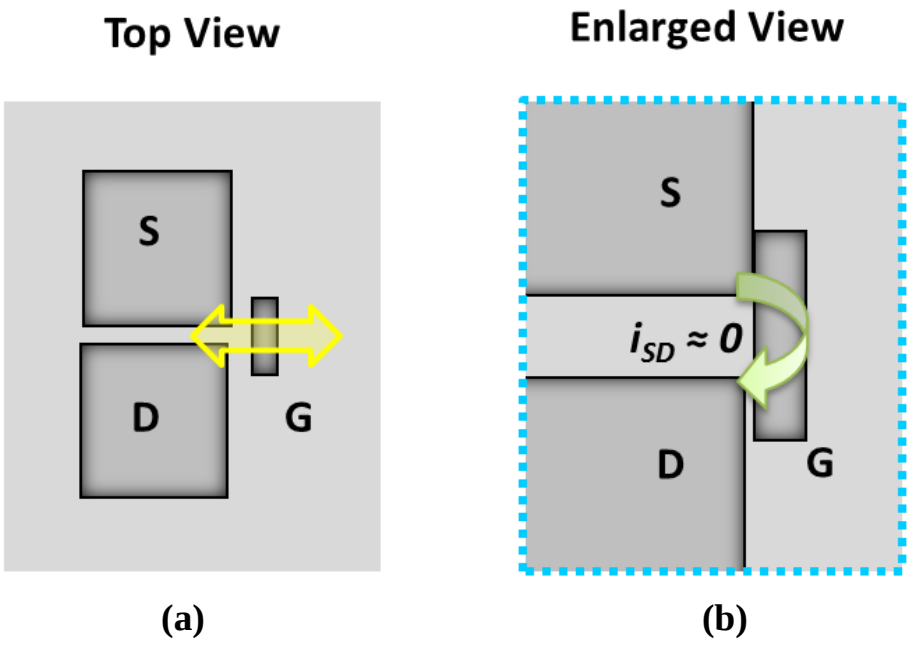


Figure 1.18: Three-terminal top-down vertical design. (a) Same operation mechanism as device in two-terminal vertical device, except electrically floating metallic island forms conduction channel between Source and Drain after actuation of pillar. (b) Enlarged view of active area after pull-in. Typical devices have surface roughness or lithography line edge roughness, resulting in nanoscale gaps. A small gap on the Source or Drain side prevents conduction.

1.6.3 Decoupling Electrical & Mechanical Properties

A single lithography top-down vertical structure has a number of interrelated parameters that simultaneously influence the electrical and mechanical attributes of the device. Figure 1.19 illustrates some of the most significant parameters that are tied to both the electrical and mechanical properties. The lithographically defined air gap determines the etch profile and depth (height) of the pillar. Wider air gaps enable better gas diffusion in narrow regions, thereby improving the aspect ratio and etch depth of the pillar. On the other hand, the air gap influences the electrostatics and the pull-in voltage of the device.

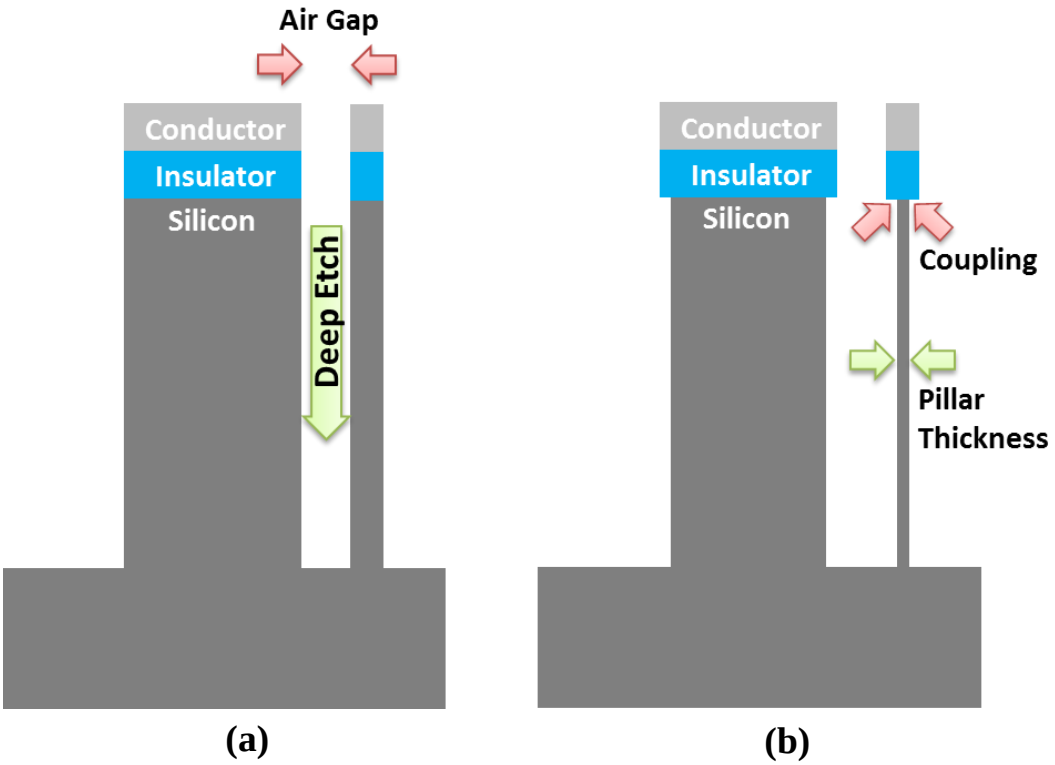


Figure 1.19: Summary of significant fabrication challenges for top-down vertical switch. Electrical and mechanical attributes generally coupled and interdependent. (a) Increased air gap enables deeper etch and higher aspect ratio pillar. However, larger air gap influences electrostatics. (b) Reduced pillar thickness reduces mechanical stiffness. However, capacitive coupling of substrate to island affected.

Another feature that impacts both the electrical and mechanical properties is the pillar thickness. A thinner pillar has low mechanical stiffness, thereby decreasing pull-in voltage. However, pillar thickness also influences the capacitive coupling of the substrate to the floating metallic island. Additionally, mechanical coupling of the pillar to the insulator is also affected by pillar thickness. Additional tradeoffs also exist. A novel solution will be presented in Chapter 2 to circumvent these fabrication related challenges. Self-aligned processes will be used to optimize the electrical and mechanical properties independently. The remainder of this thesis will discuss practical challenges and unique solutions to the previously mentioned obstacles. After presenting a thorough analysis and investigation of top-down vertical switches, device integration will be discussed along with future directions for this new class of devices.

CHAPTER 2

DESIGN OF TORSION BASED NEMS SWITCH

2.1 OVERVIEW

This chapter will discuss the operation principle unique to this vertical NEMS device. Whereas other works have focused solely on torsion [**51**] or bending [**8,19,32,48,49,54**], the work herein will elaborate on the benefits of utilizing a combination of both torsion and bending at the nanoscale. A 2-Terminal structure will be used to establish the basic operation principle of the device. Practical 3-Terminal and 4-Terminal designs will be explored. A simple theoretical model for the electrostatics and mechanics will be introduced. And this model will be used to discuss the potential scaling and optimization of the device in the context of current fabrication techniques and materials.

2.2 OPERATION PRINCIPLE OF DEVICE

The vertical NEMS device operates by means of electrostatic attraction. Most devices utilize one or more sets of parallel plates to generate an electrostatic force suitable for overcoming the bending stiffness of the cantilever or flexure system. Alternatively, fringing fields can be used with comb-drives to enable longer travel of the movable element [64]. Additionally, driving force can be independent of displacement for fixed voltage. But this comes at the expense of a lower force per unit area of the plate/electrode. Therefore a parallel plate approach is necessary for low voltage operation.

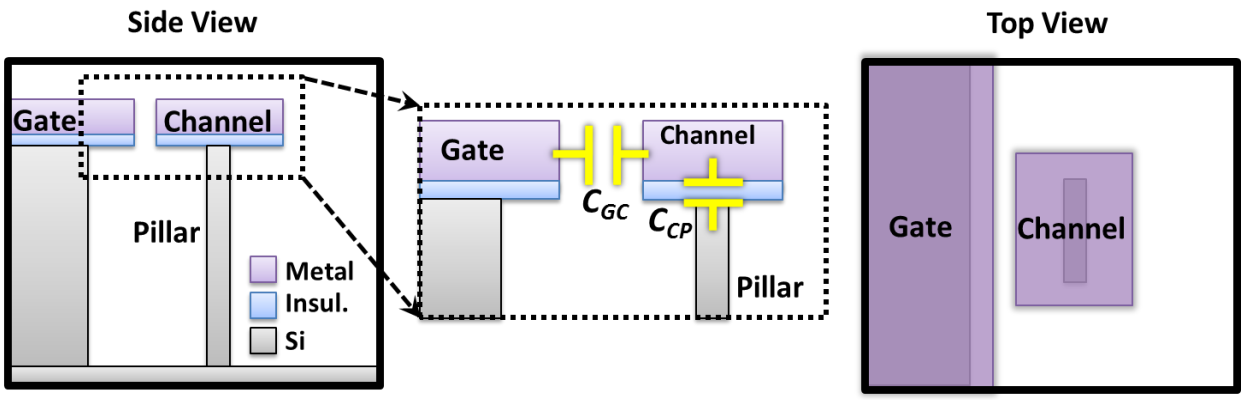


Figure 2.1: A basic schematic of the primary mode of operation using a capacitive voltage divider.

The most basic manifestation of the vertical NEMS device consists of two sets of parallel plates in series as shown in Figure 2.1. One capacitor between the Gate and Channel, C_{GC}, is defined by the two parallel metal sidewalls that are separated by an air gap. The second capacitor is between the Channel and the Pillar, C_{CP}. It is a fixed capacitance, with gap defined by an insulating thin film material. The Channel is electrically isolated, whereby its electrostatic potential is determined by the capacitive coupling of C_{GC} and C_{CP}. It should be known that a very similar looking device known as the charge shuttle or Franklin Bell operate on a different principle entirely. Whereas their symmetry requires an initial net charge on the floating conductor to initiate movement of the shuttle or an acoustic stimulus/perturbation [65], the vertical NEMS device breaks this symmetry by utilizing C_{CP} to effectively pin the voltage of the floating conductor. Therefore, the potential of the Channel is determined by the voltage division of two series capacitors, and the electrostatic force on the Channel in the direction of the Gate is proportional to the square of the voltage difference between the Gate and the Channel. Electrostatic actuation of the Channel results in bending of the pillar until pull-in occurs. In this scenario, pull-in can lead to adhesion [66]. Or alternatively, with Gate and Channel in intimate contact and effectively no potential difference between them, the Channel could pull away from

the Gate. The general limitations of a 2-terminal device were previously outlined in Chapter 1. However, a vertical nems device based on a capacitive voltage divider has an additional constraint for switching applications. The insulating spacer, i.e. fixed capacitor, eliminates the DC conduction path present for standard 2-terminal single parallel plate structures, thereby making sensing difficult even with adhesion of the channel to the gate. 3-terminal and 4-terminal designs will address this issue.

2.3 A 3-TERMINAL DESIGN

Although the primary actuation mechanism can be understood from the previous description of a simple two capacitor system, a practical switch requires a minimum of three terminals to achieve reproducible switching. In this section the structure and operation of a 3-Terminal device will be discussed and its significant drawbacks will be outlined. A 3-Terminal vertical structure can enable readout of the device state while keeping the gate electrode isolated from the conduction path.

2.3.1 Structure & Operation Principle

The 3-Terminal vertical NEMS switch can be seen as a nanorelay whereby the Channel physically connects a Source and Drain (see Figure 2.2). In this way, a low resistance metal to metal contact forms the On-state and an airgap ensures a low leakage Off-state. In this device there are two parallel capacitors in series with one capacitor to set the potential of the floating channel. Ideally the voltage of the Source and Drain will be maintained at a similar potential to limit current flow upon contact. Since the device is symmetric in voltage, the program voltage can be applied to the Body (pillar) with the Source/Drain at a low voltage or ground, or the

Source/Drain can be biased with the Body held at ground. With ideal capacitors these two scenarios should result in identical operation voltages. However, with a silicon pillar, charge depletion can cause a slight shift in operation voltage depending on the doping of the substrate. (Figure 2.3) This can become significant for aggressively scaled devices with low operation voltages. Additionally, with the current approach, all pillars are tied together electrically (Figure 2.4), thus making it more practical to bias the Soure/Drain.

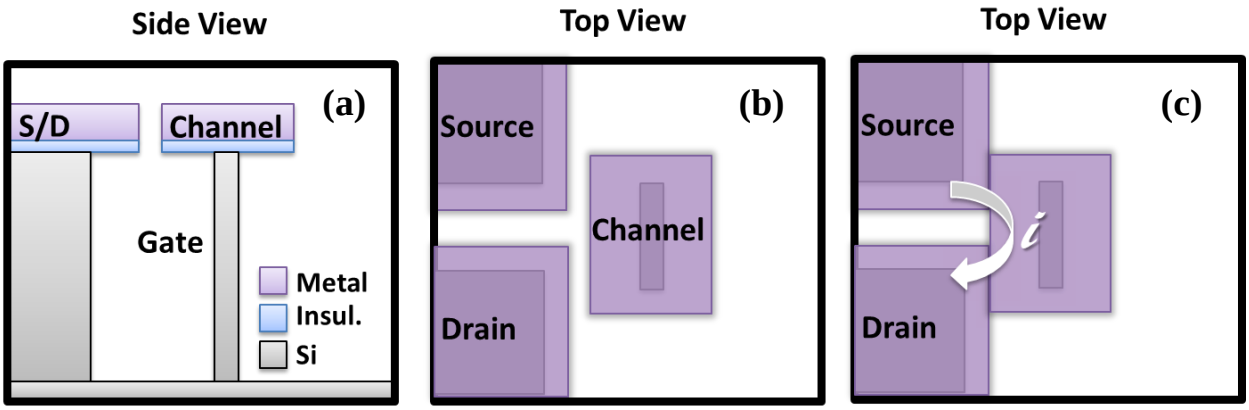


Figure 2.2: Three terminal device with pillar serving as Gate. (a) Side view of 3-terminal device retains same geometry at 2-terminal structure. (b) Top view with S and D electrodes aligned. (c) After pull-in, two low resistance metal-metal conduction channels enable electrical readout.

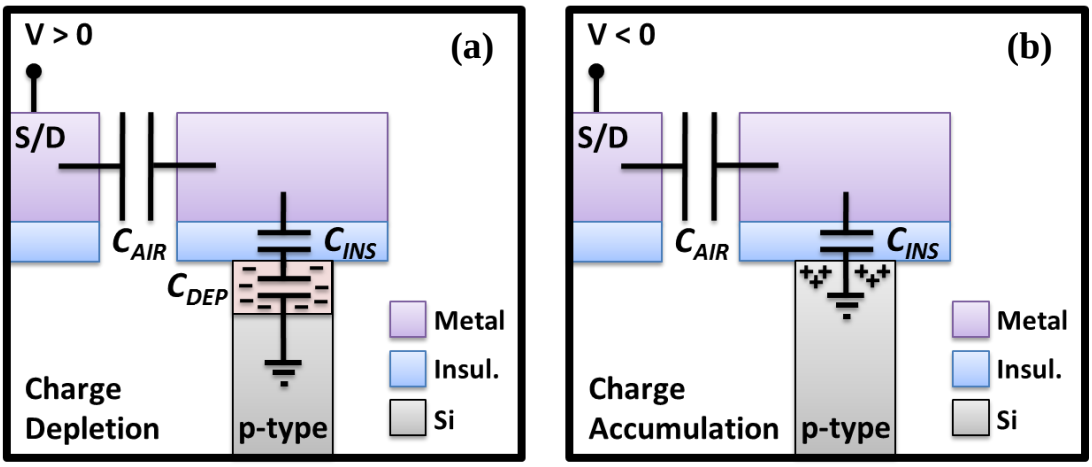


Figure 2.3: Effect of substrate doping on coupling to Channel. (a) Positive voltage on S/D causes charge depletion in substrate, and corresponding decrease in channel coupling to substrate. (b) Negate S/D voltage results in accumulation of charge in substrate.

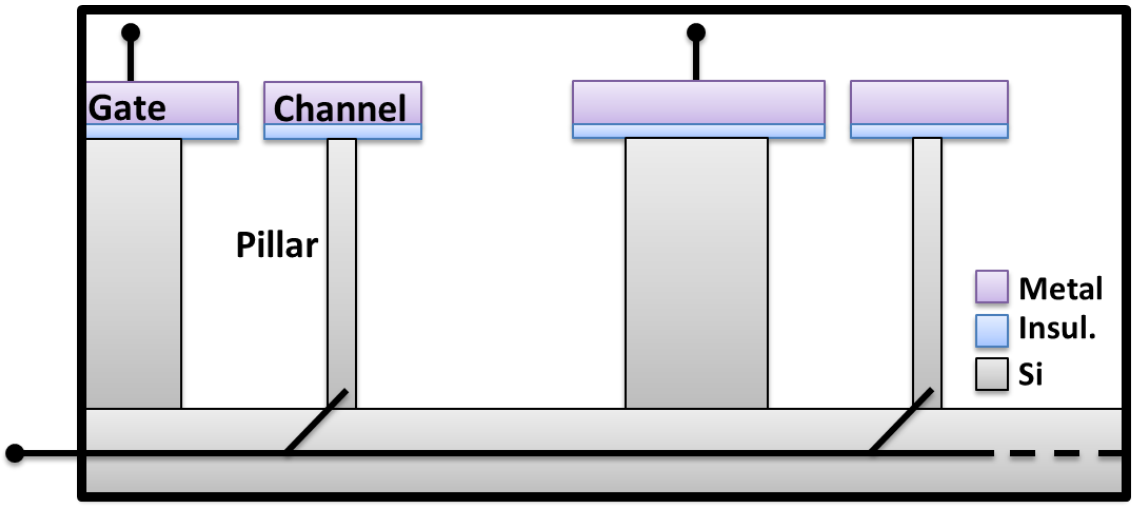


Figure 2.4: Pillars etched in bulk substrate results in common electrode for the control of the pillar potential.

2.3.2 Challenges to Reproducible Switching

The most difficult challenges to the 3-terminal design come from statistical fluctuations in lithography (line edge roughness) and metal grain roughness in thin films (Figure 2.5). Planar devices rely on the out-of-plane movement of a cantilever to form a contact with a defined electrode(s) that is directly underneath the cantilever. Therefore, a cantilever based device only has one lithographically defined electrode, and a double-clamped beam does not have a lithographically defined contact interface. (Figure 2.6) Furthermore, planar devices benefit from thin film deposition techniques including LPCVD and ALD for the interface layers, thereby decreasing the roughness of the contact area. A vertical top down fabricated device requires lithography to define the edges of the Source, Drain, and Channel from the outset of fabrication. Additionally, the simplest fabrication technique uses evaporated metal for the actual electrodes, thereby further increasing edge roughness. A 2-terminal device essentially guarantees at least one point of contact given that only one interface is necessary for operation. (Figure 2.7).

However, a 3-terminal device requires tighter tolerances for proper operation. The Channel must make simultaneous contact with both the Source and Drain in order to complete the conduction path. Whereas one contact is essentially guaranteed if pull-in is achieved, two contacts is unlikely with a simple structure given typical values for roughness. For instance, a 200 nm thick e-beam evaporated titanium film on glass can exhibit 4.9 nm ± 0.2 nm RMS surface roughness at a deposition rate of 0.5 nm/s [67]. With uncorrelated roughness at the Source and Drain electrodes, the potential exists for a local offset between the respective contacts. Offsets of this nature pose a fundamental challenge to all nano-devices and structures that require more than one point of contact for proper function. A 3-terminal vertical structure is certainly no exception. (Figure 2.8). Increasing impact velocity and repeated operation can plastically deform softer metals, such as gold, thereby partially reducing the local roughness [14]. However, for reliability and reproducible switching this solution is not satisfactory.

A simple vertical 3-terminal device uses an elongated channel of uniform width to connect the Source and Drain. The Source, Drain, and Channel are patterned in a single step of lithography. The pattern is then transferred into the substrate to define the mechanical element. Consequently, the shape of the mechanical structure mirrors the shape of the Channel, with the resulting feature being best described as a nano-ribbon. (Figure 2.9a). This ribbon-like shape has high torsional rigidity and enables only the bending mode of the device to be manifest under normal operational conditions. Upon pull-in of the Channel/ribbon, the Channel will generally make contact with only one of the electrodes. The ribbon-like shape prevents further displacement and inhibits the Channel from contacting the Source and Drain concurrently. (Figure 2.9b). Therefore, intrinsic non-uniformities in surface roughness from pattern transfer of

lithography or metal deposition result in Channel contact with either the Source or Drain only, as seen experimentally. This obstacle can be overcome naturally by a 4-Terminal device.

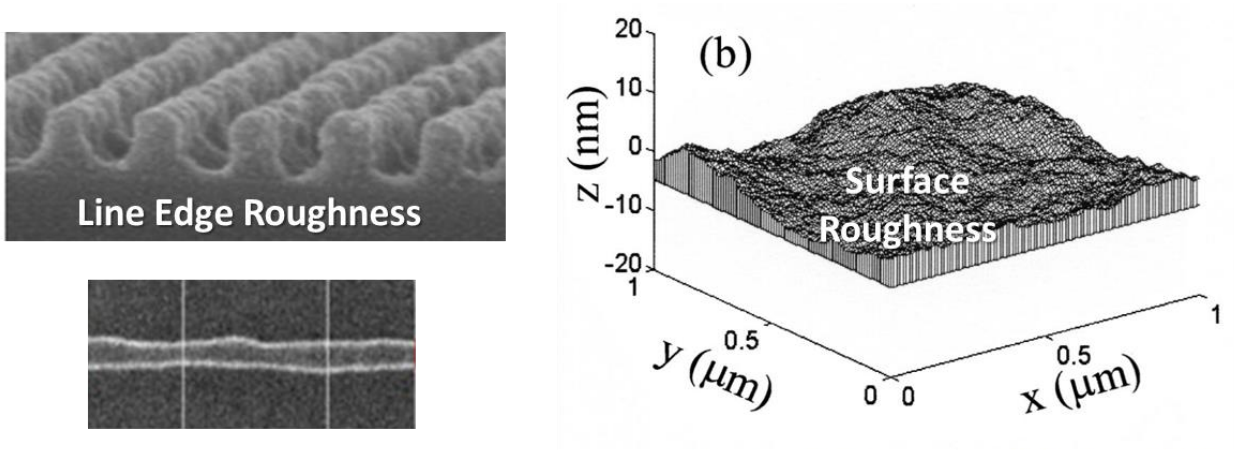


Figure 2.5: Contact surfaces are always rough. There are two main sources of roughness for nanorelays. (a) Line edge roughness from lithography. Top figure shows cross-sectional view of photoresist lines and spaces from EUV lithography. Bottom image shows top view of patterned EUV isolated line [68]. (b) Surface roughness from thin films and metallization [69].

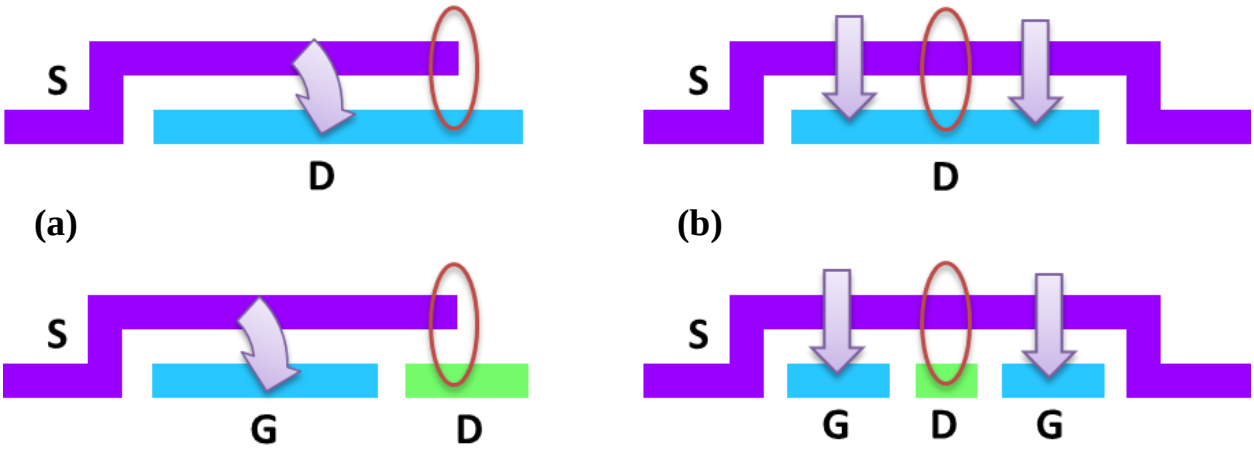


Figure 2.6: Summary of contact interfaces in planar devices. (a) 2-terminal and 3-terminal cantilever based out-of-plane planar devices have only one lithographically defined electrode. (b) 2-terminal and 3-terminal double clamped beams do not have a lithographically defined point of contact. Contact roughness is solely determined by thin film roughness.

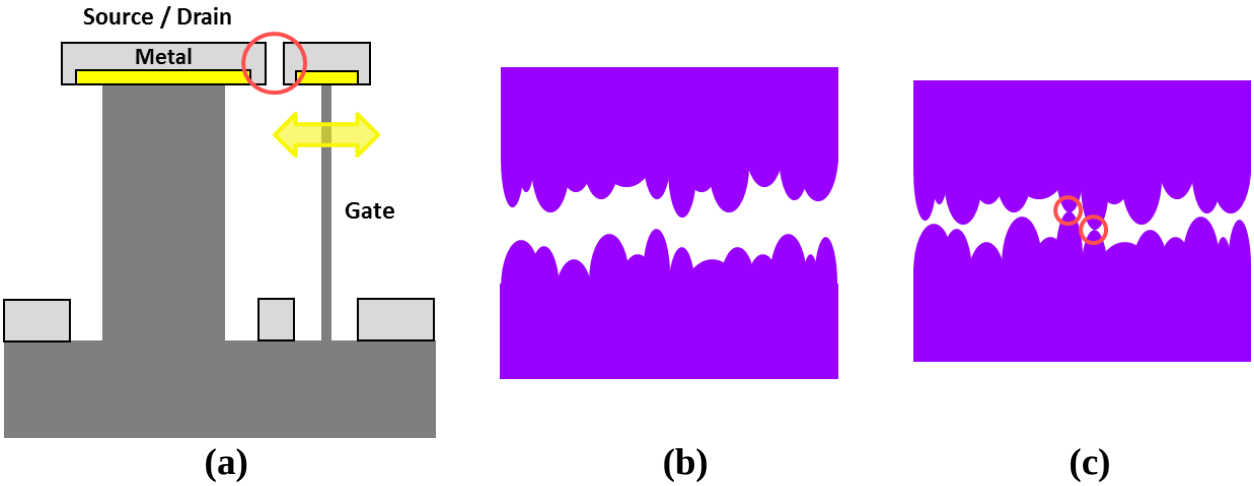


Figure 2.7: Vertical 2-terminal top down device has contributions to contact roughness from lithographically defined Source, Drain, and Channel, and evaporated metal electrodes. (a) 2-terminal structure operates in bending mode. (b) Depiction of contact surfaces with roughness prior to pull-in. (c) Depiction of contact surfaces after pull-in with two points of intimate contact.

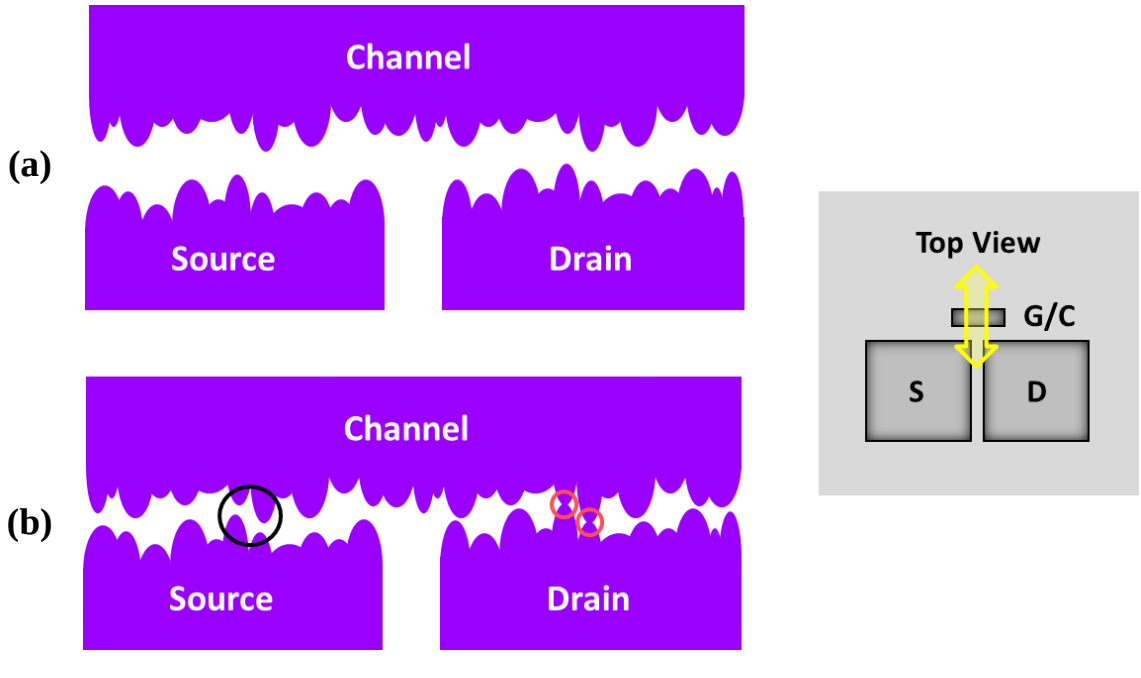
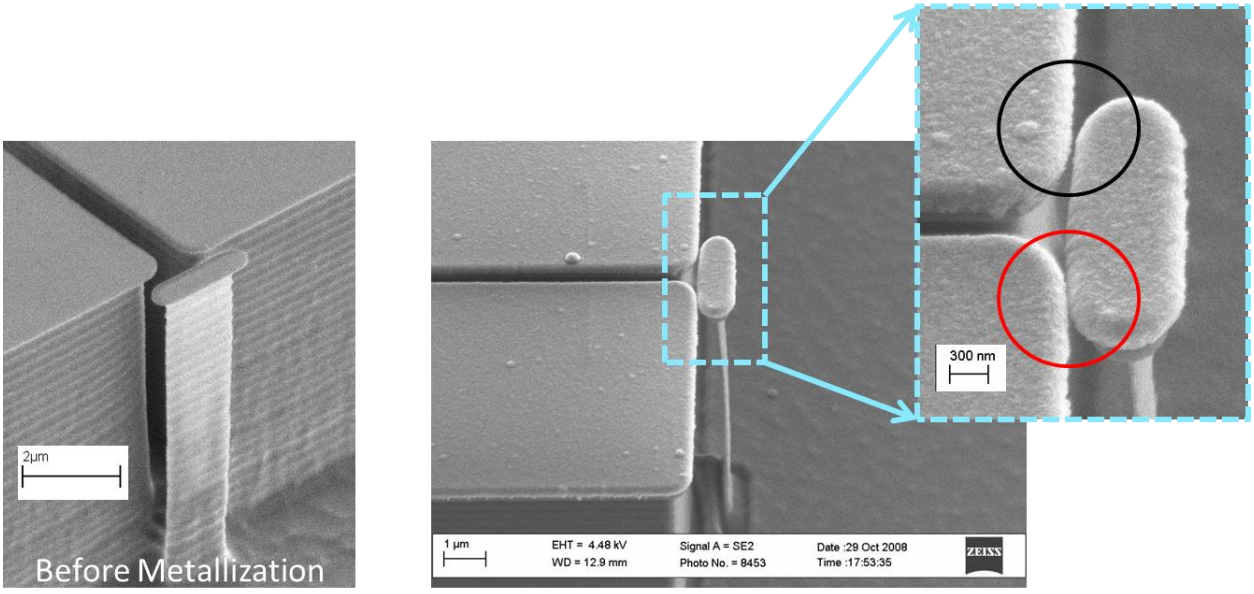


Figure 2.8: Depiction of roughness in a 3-terminal device. (a) Device before actuation. (b) Device after actuation. Typical device will make contact with only the Source or Drain under normal operation conditions, assuming a bending mode of actuation (no torsion).



(a) **(b)**

Figure 2.9: A fabricated vertical top-down 3-terminal device in silicon. (a) Channel, Source, and Drain patterned in single lithography. All subsequent processing self-aligned. Channel shape is transferred into silicon substrate, thereby making a nano-ribbon structure. (b) Typical device after metallization. Ribbon structure with high torsional rigidity prevents correction for roughness. SEM image of device with only one contact successfully achieved.

2.4 A 4-TERMINAL DEVICE DESIGN

A fourth terminal is introduced between the Source and Drain terminals as seen in Figure 2.10. Additionally, the nanoribbon design of the three-terminal device is replaced by a nanopillar design for the four-terminal structure. The inclusion of the Gate terminal combined with the nanopillar structure enhances device functionality and enables torsion to augment the bending operation. This section will discuss the design of 4-Terminal devices and their advantages over 3-Terminal designs. Specific attention will be given to the benefits of torsional operation.

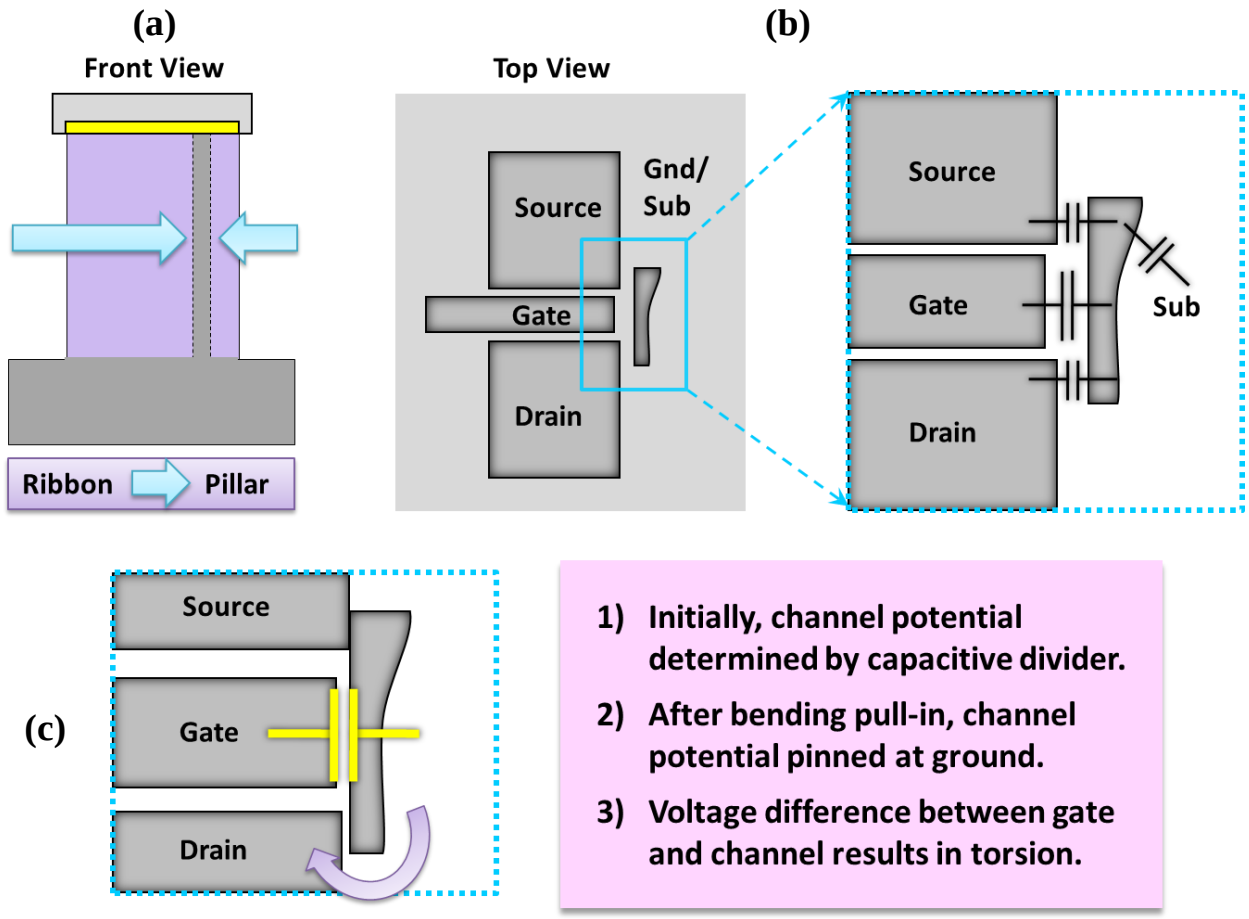


Figure 2.10: Schematic of 4-terminal device and basic operation mechanism, as compared to a 3-terminal device. (a) Transition from nano-ribbon structure to nano-pillar structure. Nano-pillar is offset to side to increase torque of electrostatic force on Channel. (b) 4-terminal device has similar capacitive divider operation to 3-terminal device. Before initial pull-in, operation is primarily in bending mode. (c) After bending pull-in, if device does not make contact with both Source and Drain electrodes simultaneously, device operates similar to a 3-terminal structure. However, force on Channel determined by a single parallel plate capacitor, with a small air gap between Gate and Channel. Channel will experience a torque, whereby Channel will achieve simultaneous contact of Source and Drain.

2.4.1 Bending Operation

The bending mode of operation of the 4-Terminal device functions similarly to its 3-Terminal predecessor. The primary difference is the additional capacitance between the Gate terminal and the Channel, C_{GC}. This capacitance serves a critical role in isolating the potentially detrimental effects of the Source/Drain voltages. The 3-Terminal device relies on the Source and

Drain voltages to set the biasing conditions for the pull-in condition. And in order for the pull-in condition to be reached, there must be a sufficient voltage difference between the Source/Drain voltages and the Pillar, i.e. Ground. Therefore, the Source/Drain voltages must be constrained while programming the switch to enable proper operation. In short, the electrodes used for contact are the very same electrodes that fix the floating potential of the Channel. The 4-Terminal device partially decouples these two roles, thereby making a practical switch that is much more feasible to integrate with current CMOS technology.

Before initial pull-in, operation is primarily in the bending mode. Therefore, the 4-terminal device operates in a similar fashion to the 3-terminal structure, whereby the potential of the Channel, and the pull-in voltage are determined by a capacitive voltage divider. The main difference is that four capacitances couple to the Channel rather than three. Additionally, the newly introduced Gate electrode between the Source and Drain must be slightly recessed to avoid contact with the Channel after pull-in is achieved. After pull-in due to bending, if the device does not make contact with both the Source and the Drain electrodes simultaneously, the device automatically transforms to a 3-terminal structure.

2.4.2 Torsional Operation

When the Channel makes contact with either the Source or Drain electrode, intimate contact of a metal-metal interface sets the potential of the Channel, thereby eliminating the electrostatic influence of the Pillar. The force on the Channel is then determined by a single parallel plate capacitor. A small air gap between the Gate and Channel, approximately equal to the lithographically defined offset of the Gate from the Source/Drain, establishes an electrostatic force on the Channel. With the entire Gate voltage dropping across the air gap, as opposed to the

case with the capacitive voltage divider, the electrostatic force on the Channel is enhanced after initial pull-in, assuming the Source/Drain are grounded. (Figure 2.10). The device resembles other 3-terminal structures described in Chapter 1 [37][53][54] when the Channel is in contact with either the Source or Drain. However, the mechanical stiffness of the structure for secondary pull-in, after bending pull-in, is not due to the stiffness of the Channel, but rather the torsion stiffness of the nano-pillar. This enables the device to operate at a much lower voltage than other "lateral" 3-terminal devices of similar dimensions. Therefore, after bending pull-in, the Channel will experience a torque, and undergo torsional pull-in, whereby the Channel will achieve simultaneous contact of the Source and Drain. If the voltage for bending pull-in is higher than that of the torsional pull-in, switching will be achieved when the bending pull-in voltage is applied. However, if the torsional pull-in voltage is higher, bending pull-in can be achieved without turning on the switch. In either case, the switching characteristics will appear abrupt, with no indication of a primary and secondary contact, since no Source-Drain current flows until the Channel makes simultaneous contact with both electrodes.

2.5 CAPACITIVE COUPLING

An overview of the relevant capacitances will be presented. An analytical model for the 3-terminal nano-ribbon device will be discussed. Practical assumptions are imposed to reach an expression for operation voltage of the structure in terms of all the relevant design parameters. 3- and 4-terminal devices are compared, with thought given to extending the 3-terminal analysis to the 4-terminal structure.

2.5.1 Voltage Division & Simple Capacitive Model

In terms of the capacitances, the 3-Terminal device has C_{SC} and C_{DC} in parallel, with the Source and Drain each contributing half the parallel capacitance to the Channel, and combined they are approximately equal to the Pillar capacitance to the Channel, C_{PC}. However, with the 4-Terminal device, the Gate capacitance to the Channel, C_{GC}, becomes the primary capacitance besides C_{PC}, with C_{SC} and C_{DC} being marginalized in the bending mode of operation. Ideally the overlap of the Source and Drain with the Channel should be minimized to further decrease undesirable coupling. This in turn increases the ability of C_{GC} and C_{PC} to control the potential of the Channel. However, the Source and Drain must have some overlap with the Channel in order to assure that contact will be achieved when the Channel undergoes pull-in. Therefore, the Source and Drain must be in the trajectory of the Channel.

The figure of merit for nano-relays is the turn on voltage, or the voltage at which a high impedance channel becomes conducting by mechanical means. The turn on voltage for electrostatic actuators is synonymous with the pull-in voltage of the device. Therefore, it is useful to have an expression for the pull-in voltage of the device in terms of the mechanical and electrical properties of the structure. The analysis uses a quasi-static assumption for the Gate voltage, where the voltage is increased slowly until the device turns on and contact is achieved. To solve the bending problem analytically for the 3-terminal nano-ribbon device, it is also necessary to assume that the Source and Drain are grounded during programming. This simplifies the problem by allowing C_{SC} and C_{DC} to be in parallel, for a total equivalent capacitance $C_T = C_{SC} + C_{DC}$. This reduces the problem so that the floating potential can be determined by the voltage divider of the series capacitances, C_T and C_{GC}. As discussed in the

previous paragraph, it cannot always be assumed that the Source and Drain voltages are grounded during programming, but there is much to be learned from this scenario.

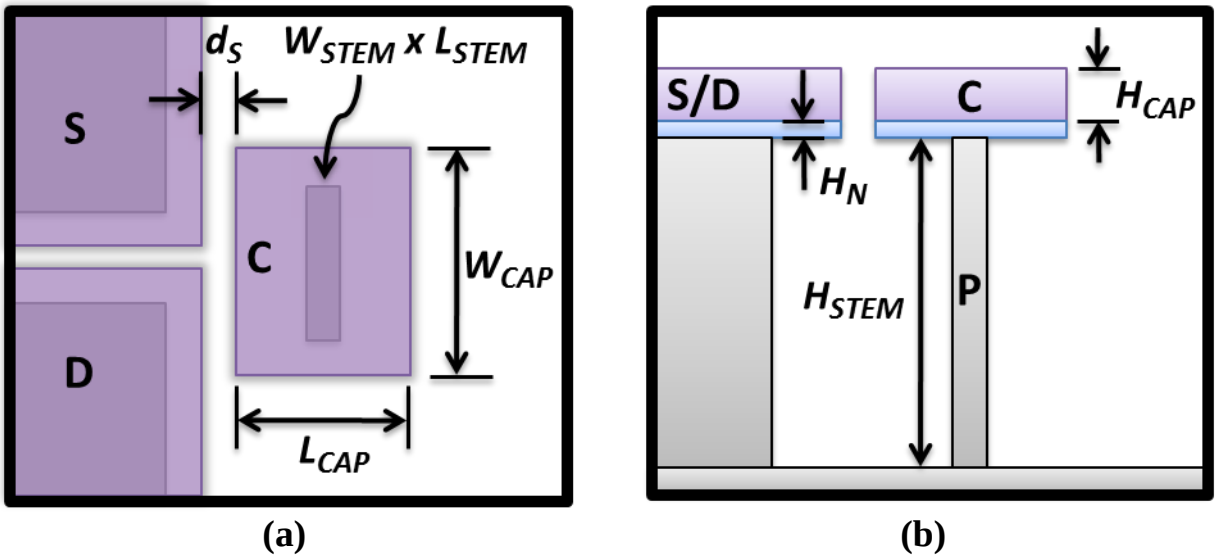


Figure 2.11: Schematic for determining analytical model of device operation and scaling. (a) Top view of 3-terminal nano-ribbon device. W_{STEM} and L_{STEM} are the width and length of the pillar underneath the Channel. (b) Side view of vertical structure.

With Source and Drain biased at 0V, an analytical model can be determined for the structure when the fringing fields are negligible. Using Figure 2.11 to form a simple model, the potential of the floating Channel, C, can be evaluated in terms of the applied voltages and capacitances. It is assumed that the floating Channel is initially charge neutral, Q = 0, which gives the following expression:

$$C_G(V_C - V_G) + C_S(V_C - V_S) + C_D(V_C - V_D) = 0 \tag{2.1}$$

Solving for the unknown floating potential on the Channel, with $C_S = C_D$, and $V_S = V_D = 0$:

$$V_C = \frac{C_G}{C_G + C_S + C_D} V_G = \frac{C_G}{2C_S + C_G} V_G \tag{2.2}$$

Now, the horizontal component of the force on the Channel produces a non-zero bending moment on the ribbon. It is assumed that the gap between the Source and Drain is small compared to the width of the Channel, W_{CAP}, so that the area of the capacitance considered for the electrostatic force is roughly H_{CAP} by W_{CAP}. Using Equation 2.8 for the attractive electrostatic force of a parallel plate capacitor, an expression can be written for the force that the Source and Drain exert on the Channel, with $V_S = V_D$:

$$F_E = \frac{\varepsilon_0}{2}\frac{H_{CAP}W_{CAP}}{d_S^2}(V_C - V_S)^2 \tag{2.3}$$

By substituting Equation 2.2 for V_C, defining $C_0 = \varepsilon_0 H_{CAP} W_{CAP}$, and setting $V_S = 0$, we can write the electrostatic force in terms of the applied voltage, V_G, and the relevant capacitances:

$$F_E = \frac{C_0}{2d_S^2}\left(\frac{C_G}{2C_S + C_G}\right)^2 V_G^2 \tag{2.4}$$

And with $C_S \approx C_0/2d_S$, $d_0 = C_0/C_G$, where $C_G = \kappa\varepsilon_0 W_{STEM} L_{STEM}/H_N$:

$$F_E \approx \frac{C_0 V_G^2}{2(d_0 + d_S)^2} \tag{2.5}$$

Finally we need to consider the displacement of the Channel away from its equilibrium position. If x is the displacement of the Channel in the direction of the Source and Drain, then the gap between the Channel and the Source/Drain becomes $d_S - x$. Therefore, by replacing d_S with $d_S - x$, we have a relationship for the electrostatic force on the Channel as a function of position:

$$F_E(x) \approx \frac{C_0 V_G^2}{2(d_0 + d_S - x)^2} \tag{2.6}$$

The mechanical restoring force opposes the electrostatic force, as discussed in Section 2.2. The mechanical restoring force is given by:

$$F_M(x) = -k_M x = -\frac{E W_{STEM} L_{STEM}^3}{4H_{STEM}^3} x \tag{2.7}$$

The pull-in condition occurs when an instability is encountered between the quadratic electrostatic force and the linear-elastic restoring force. The pull-in voltage can be found by determining the value of V_G for which $F_E(x)$ is tangential to $F_M(x)$. The condition of tangency can be solved with the following two expressions given by $F_M(x) = F_E(x)$, and $\frac{dF_M}{dx} = \frac{dF_E}{dx}$:

$$k_M x = \frac{C_0 V_G^2}{2(d_0 + d_S - x)^2} \tag{2.8}$$

$$k_M = \frac{C_0 V_G^2}{(d_0 + d_S - x)^3} \tag{2.9}$$

Therefore, the point of tangency is given by $x = (d_0 + d_S)/3$. And pull-in will only occur if $d_S > (d_0 + d_S)/3$, or $2d_S > d_0$. In terms of the specific device parameters, the critical initial gap for the pull-in condition is given by:

$$d_S > \frac{H_{CAP} W_{CAP} H_N}{2\kappa L_{STEM} W_{STEM}} \tag{2.10}$$

Consequently, if the initial gap between the Channel and the Source/Drain is less than this critical gap, the switch will make contact without experiencing the pull-in condition. Turn-on of the switch will still be instantaneous when contact is made to the Source and Drain, however, actuation of the Channel will be smooth, and the Channel will traverse the Source/Drain gap without undergoing the rapid acceleration characteristic of the pull-in condition. For a typical configuration, with $H_{CAP} = 400\ nm, W_{CAP} = 2.5\ \mu m, H_N = 125\ nm, \kappa = 7.5, L_{STEM} = 100\ nm$, and $W_{STEM} = 2.1\ \mu m$, the critical initial gap would need to be less than or equal to *39.7 nm* to avoid the pull-in condition. This would be a rather small gap in comparison with the scale of the other dimensions. The critical initial gap can be tailored in accordance with Equation 2.10 by increasing parameters in the numerator or decreases those in the denominator; however, the overall effect would tend to increase the operation voltage. Depending on the application and the

voltage and reliability requirements, a device could potentially be designed without the pull-in effect. Although this is not possible with a single capacitor device, a device based on a capacitive voltage divider can intrinsically avoid pull-in. The fixed series capacitance, C_G, provides negative feedback to stabilize the device. Since the device is naturally a capacitive voltage divider, if the Channel begins to pull-in, the variable capacitor, C_S, increases, thereby causing a corresponding decrease in the voltage across it. Therefore, this passive negative feedback can help mediate the pull-in effect [6]. Depending on the value of the fixed series capacitor, a shift is affected in the electrostatic force curve so that the point of instability is reached only at larger displacements from equilibrium. And for an appropriate choice of capacitance the pull-in instability is completely avoided. If the device operates in the pull-in regime, then the pull-in voltage is given by:

$$V_G^{pull} \approx \sqrt{\frac{8(d_0 + d_S)^3 k_M}{27 C_0}} \tag{2.11}$$

And in terms of the relevant device parameters:

$$V_G^{pull} \approx \sqrt{\frac{2EW_{STEM}L_{STEM}^3\left(\frac{H_{CAP}W_{CAP}H_N}{\kappa L_{STEM}W_{STEM}} + d_S\right)^3}{27\varepsilon_0 H_{CAP}W_{CAP}H_{STEM}^3}} \tag{2.12}$$

And if the switch does not fulfill the pull-in condition, then the operation voltage can be found by setting $F_M(x \to d_S) = F_E(x \to d_S)$:

$$V_G^{contact} \approx \sqrt{\frac{2d_0^2 k_M d_S}{C_0}} \tag{2.13}$$

And in terms of the relevant device parameters:

$$V_G^{contact} \approx \sqrt{\frac{EL_{STEM}H_{CAP}W_{CAP}H_N^2 d_S}{2\kappa^2\varepsilon_0 H_{STEM}^3 W_{STEM}}} \tag{2.14}$$

2.5.2 Operation Voltage with Side Gate

Adding an additional Side Gate on the opposite side of the Channel can potentially enhance the operation of the device. A Side Gate has been employed as a counter electrode to help overcome the challenges of stiction [70]. We can analyze the effect of the Side Gate on the overall operation voltage of the device. Using a revised version of Figure 2.11 with a Side Gate, we can perform a similar analysis to that of Section 2.5.1 to find the operation mode and voltages.

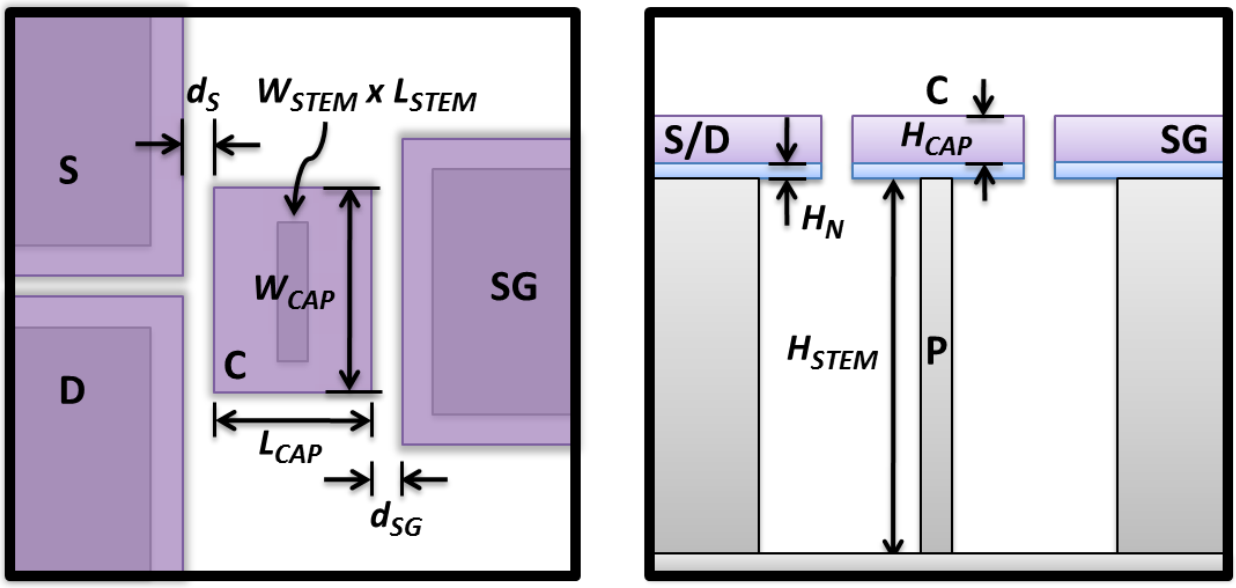


Figure 2.12: Schematic for determining operation voltage device with the additional influence of a Side Gate. (a) Top view of 3-terminal device with Side Gate on the opposite side of the Channel from the Source/Drain. (b) Side View of vertical structure with Side Gate.

We can write an expression to find the potential of the Channel as we did with Equation 2.1, where the Channel is assumed to be initially charge neutral:

$$C_G(V_C - V_G) + C_S(V_C - V_S) + C_D(V_C - V_D) + C_{SG}(V_C - V_{SG}) = 0 \qquad (2.15)$$

Solving for the unknown floating potential on the Channel, with $C_S = C_D$, $V_S = V_D = 0$, and assuming that $V_{SG} = V_G$:

$$V_C = \frac{C_G + C_{SG}}{C_G + C_{SG} + C_S + C_D} V_G = \frac{C_G + C_{SG}}{C_G + C_{SG} + 2C_S} V_G \tag{2.16}$$

V_{SG} and V_G are the applied Side Gate and Gate voltages respectively. Ideally, the Side Gate potential should be the same as the floating potential of the Channel during pull-in or contact. If there is a potential difference between them, then there will an electrostatic force on the Channel opposing the attractive force of the Source/Drain, thereby increasing the operation voltage of the device. Use of the electrostatic force of the Side Gate is best reserved for operation after pull-in, when the additional electrostatic force can assist the mechanical restoring force if stiction is prevalent. If the Source/Drain gaps are equal to the Side Gate gap, keeping the Side Gate grounded would result in the least favorable situation, essentially no net force on the Channel. And in a more likely scenario, the same voltage can be applied to the Side Gate and Gate. We can then write an expression for the net electrostatic force on the Channel:

$$F_E = \frac{\varepsilon_0}{2} \frac{H_{CAP} W_{CAP}}{d_S^2} (V_C - V_S)^2 - \frac{\varepsilon_0}{2} \frac{H_{CAP} W_{CAP}}{d_{SG}^2} (V_C - V_{SG})^2 \tag{2.17}$$

We then substitute Equation 2.16 for V_C, $V_{SG} = V_G$, and $V_S = 0$:

$$F_E = \frac{\varepsilon_0}{2} H_{CAP} W_{CAP} \left(\frac{V_G}{C_G + C_{SG} + 2C_S} \right)^2 \left[\left(\frac{C_G + C_{SG}}{d_S} \right)^2 - \left(\frac{2C_S}{d_{SG}} \right)^2 \right] \tag{2.18}$$

Next, with $C_0 = \varepsilon_0 H_{CAP} W_{CAP}$, we can express:

$$C_{SG} \approx \frac{C_0}{d_{SG} + x} \qquad and \qquad C_S \approx \frac{1}{2} \frac{C_0}{d_S - x} \tag{2.19}$$

By replacing d_S by $d_S - x$ and d_{SG} by $d_{SG} + x$ to account for position dependence of the force on the Channel, and assuming that the Source/Drain gap is equal to the Side Gate gap, $d_{SG} \approx d_S = d$,

defining $d_0 = C_0/C_G$, we can write a simple expression for the electrostatic force on the Channel as a function of position:

$$F_E = \frac{C_0}{2} V_G^2 \frac{(d+x)(2d_0+d+x)}{(2dd_0+d^2-x^2)^2} \tag{2.20}$$

If we let:

$$f(x) = \frac{(d+x)(2d_0+d+x)}{(2dd_0+d^2-x^2)^2} \tag{2.21}$$

We can solve the pull-in condition as before:

$$k_M x = \frac{C_0 V_G^2}{2} f(x) \tag{2.22}$$

$$k_M = \frac{C_0 V_G^2}{2} f'(x) \tag{2.23}$$

This requires us to solve:

$$x f'(x) = f(x) \tag{2.24}$$

Which we can simply write as:

$$\frac{1}{d+x} + \frac{1}{d+x+2d_0} + \frac{4x}{2d_0 d + d^2 - x^2} = \frac{1}{x} \tag{2.25}$$

And this can be re-written as a quartic:

$$3x^4 + 8(d+d_0)x^3 + 6d(d+2d_0)x^2 - d^2(d+2d_0)^2 = 0 \tag{2.26}$$

Equation 3.26 can then be numerically solved for the position at which the Channel undergoes pull-in. The following expression can then be used to fit the numerical solution:

$$x_{pull} = \frac{\sqrt{d(d+2.16d_0)}}{3} - 0.0265d_0 \tag{2.27}$$

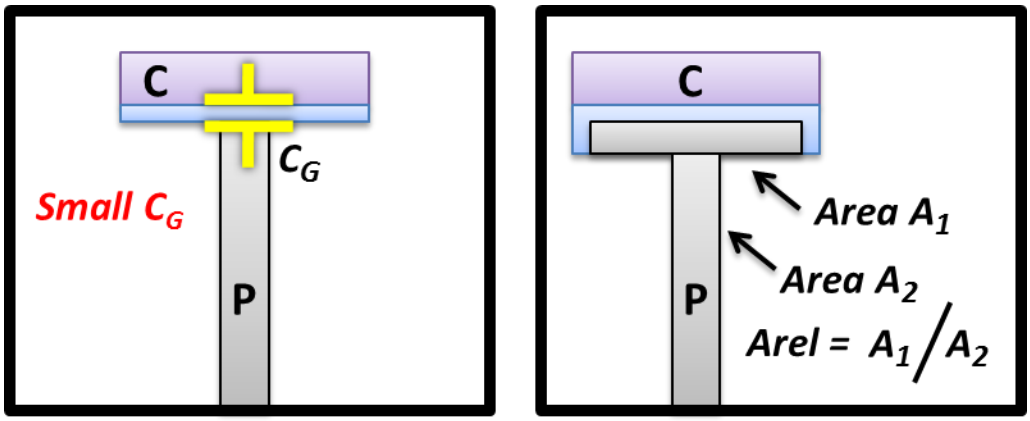
Similarly, another expression can be used to fit the numerical solution to the pull-in voltage of the device for values of *d* and d_0 that give solutions within the pull-in regime:

$$V_G^{Pull} = \sqrt{\frac{k_m d^3}{4C_0}}\left(\sqrt{1 + 3.6\frac{d_0}{d}} + 0.285\frac{d_0}{d}\right) \tag{2.28}$$

We can now evaluate this expression and compare it to the device without a side gate for a structure with $H_{CAP} = 400\ nm, W_{CAP} = 2.5\ \mu m, H_N = 125\ nm, \kappa = 7.5, L_{STEM} = 100\ nm,$ $W_{STEM} = 2.1\ \mu m,\ H_{STEM} = 10\ \mu m,\ d = 150\ nm,$ and $E = 110\ GPa$. For these values, d_0 = *79.4 nm*, k_m = *0.058 N/m*, and C_0 = *8.85 x* 10^{24} *F·m*. V_{Pull} = *1.71V* without a Side Gate, and V_{Pull} = *4.36V* with a Side Gate. Therefore, the Side Gate has quite a dramatic effect on the pull-in voltage of the device. It may be undesirable to include the Side Gate for low voltage operation, although the challenge of stiction will still need to be addressed.

2.5.3 Increased Capacitive Coupling from Gate/Pillar, A_{rel}

Upon further examination of the structure we have analyzed up until this point, a significant enhancement in performance becomes possible with a slight modification of the design. Since the ribbon or pillar is designed to be compliant, L_{STEM} X W_{STEM} can be quite small compared to L_{CAP} X W_{CAP}, as determined by the fabrication procedure. However, when the pillar dimensions are small compared to the Channel dimensions, capacitive coupling is reduced, and the Gate/Pillar weakly couple to the Channel. To increase the control of the Gate/Pillar, it is necessary to maintain a larger area of coupling. In a silicon based device, a thin silicon layer would need to be retained under the entire Channel, as depicted in Figure 2.13.



(a) **(b)**

Figure 2.13: Schematic of benefit of increased capacitive coupling between Pillar and Channel. (a) Capacitance of original design limited by dimensional requirements of mechanical pillar. (b) Capacitive coupling of Pillar to Channel can be increased while maintaining the stiffness of the Pillar, thereby decoupling the electrostatics and mechanics.

The advantage can be analyzed by exchanging $L_{STEM}\ W_{STEM}$ by $A_{rel}\ L_{STEM}\ W_{STEM}$, within the term in Equation 2.12 that accounts for the effect of C_G:

$$V_G^{pull} \approx \sqrt{\frac{2EW_{STEM}L_{STEM}^3\left(\frac{H_{CAP}W_{CAP}H_N}{\kappa \boldsymbol{A_{rel}} L_{STEM}W_{STEM}} + d_s\right)^3}{27\varepsilon_0 H_{CAP}W_{CAP}H_{STEM}^3}} \tag{2.29}$$

This silicon layer serves an additional mechanical purpose by increasing the overall stiffness of the Channel, thereby eliminating any deleterious stress effects from the thick metallization for the Channel. And most importantly, this layer effectively decouples the electrical and mechanical aspects of the device. Previously, a smaller pillar meant a corresponding decrease in coupling to the Channel. Now both the electrostatics and mechanics can be optimized independently. Further attention will be given to the benefits of A_{rel} during the discussion on scaling.

2.5.4 Simulation of Electrostatics

The electrostatics of the 4-terminal device are slightly more complicated because the gap between the Source/Drain and the Channel is smaller than the gap between the Gate and the Channel by ~ 100nm. The gate must be recessed to prevent shorting of the Gate to the Channel during operation. For further analysis, the finite element method (FEM) was employed using COMSOL Multiphysics. The simulations enabled us to evaluate the electrostatic force on the Channel while accounting for non-parallel capacitive plates, and lithographically defined electrodes with rounded corners.

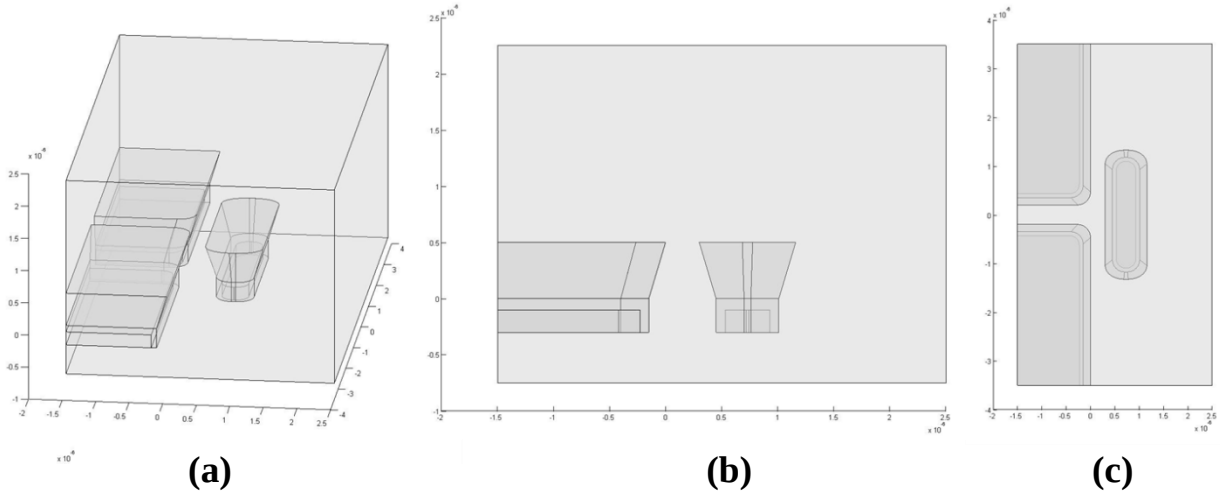
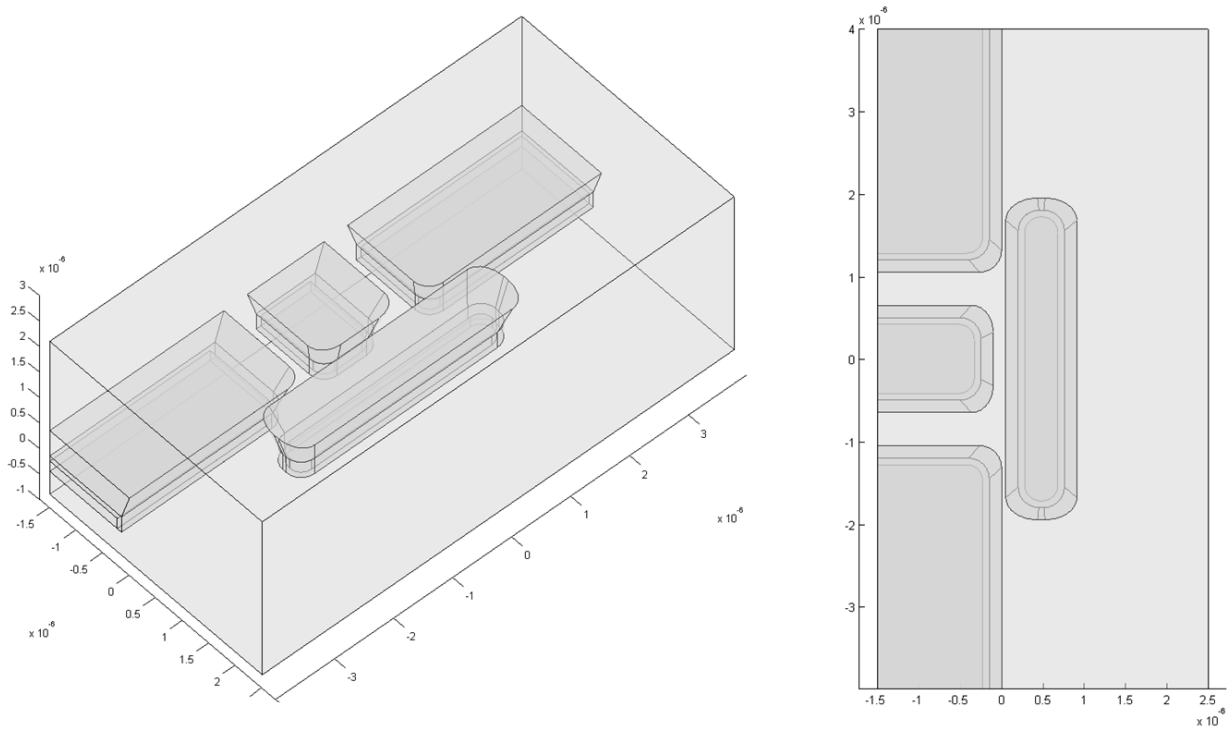


Figure 2.14: Schematic of 3-terminal device simulated in COMSOL Multiphysics. (a) 3-D perspective of structure used to simulate electrostatics. (b) Side view of device showing non-parallel capacitive plates, and increased coupling from the pillar (A_{rel}). (c) Top view of device showing electrodes with rounded corners.

The electrostatics of a 3-terminal device, as shown in Figure 2.14, were simulated to verify the theoretical model developed in section 2.5.1, and for a point of comparison to the 4-terminal device. A 4-terminal device was analyzed, as shown in Figure 2.15, and the electrostatic force was extracted from the simulation. The simulation of a 4-terminal device is generally performed with $V_G = 1V$, and $V_S=V_D=V_P=0V$. The electrostatic force on the Channel

is evaluated as a function of gap size between the Channel and the Source/Drain. A gap of 0 nm corresponds to the onset of contact between the Channel and the Source/Drain. The curve can then be fit by Expression 2.6, with d_0 and C_0 as the fitting parameters, as shown in Figure 2.16. Ultimately, the pull-in voltage can be calculated using the values for these fitting parameters in Equation 2.11, with a known initial gap size, d_S, and a calculated or simulated mechanical spring constant for the pillar, k_M.



(a) **(b)**

Figure 2.15: 4-terminal electrode design for simulation in COMSOL. (a) 3-D perspective of structure used to analyze electrostatics. (b) Top view of device showing Gate offset from Source and Drain. Image depicts Channel almost in contact with Source and Drain.

FEM analysis was also used to assess the relative magnitude of the effect of various design changes on the electrostatic force. Figure 2.17 summarizes the most significant changes to design. The device started without torsion, and received a boost in force when switching to

the torsion-based design. The primary reason for increase in force can be seen from Equation 2.6. In order to incorporate the Gate between the Source and Drain in a torsion-based device, the Channel width, W_{CAP}, had to be increased to allow for gaps between the Gate and both the Source and Drain, and the added width of the Gate. In this case, the potential of the Channel will remain relatively unchanged because the two primary capacitors in the capacitive voltage divider change proportionately with an increase in Channel width, assuming a conducting layer is maintained under the entire Channel, as described in Section 2.5.3. Therefore, the d_0 term in Equation 3.6 remains relatively constant ($d_0 = C_0/C_P$). However, the numerator, which takes into account the horizontal component of force, increases with an increase in W_{CAP}. However, the increase in force for a torsion-based structure assumes the Gate, Source, and Drain to be collinear and aligned. In a practical device, the Gate must be recessed from the Source and Drain to prevent shorting of the Gate to the Channel, as seen in Figure 2.15. A 100 nm offset for the Gate results in a substantial decrease in the force on the Channel, to less than that of the original nano-ribbon device. In this scenario, the overall distance between the moveable Channel and the fixed Gate electrode increases, thereby decreasing the capacitive coupling of the Gate to the Channel, and lessening the Gate's control of the Channel. One additional scenario is simulated, whereby the Pillar coupling to the Channel is reduced to the cross-sectional area of the pillar, rather than the entire area of the Channel (i.e. no A_{rel}). The force on the Channel further decreases in this case, as seen from Equation 2.6. The d_0 term in the denominator increases, because C_P decreases with decreased coupling to the Channel.

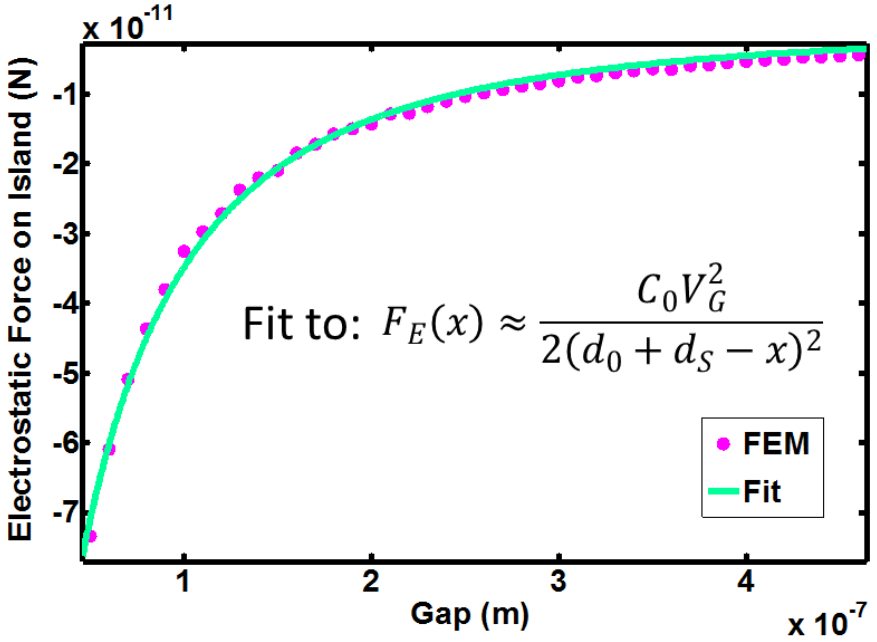


Figure 2.16: Typical electrostatic force curve for 4-terminal device. Curve is generated with $V_G = 1V$, and $V_S = V_D = V_P = 0V$. Position of the Channel is changed with respect to the Source/Drain, and electrostatic force on Channel is evaluated at each point. Gap = 0 nm corresponds to condition of contact.

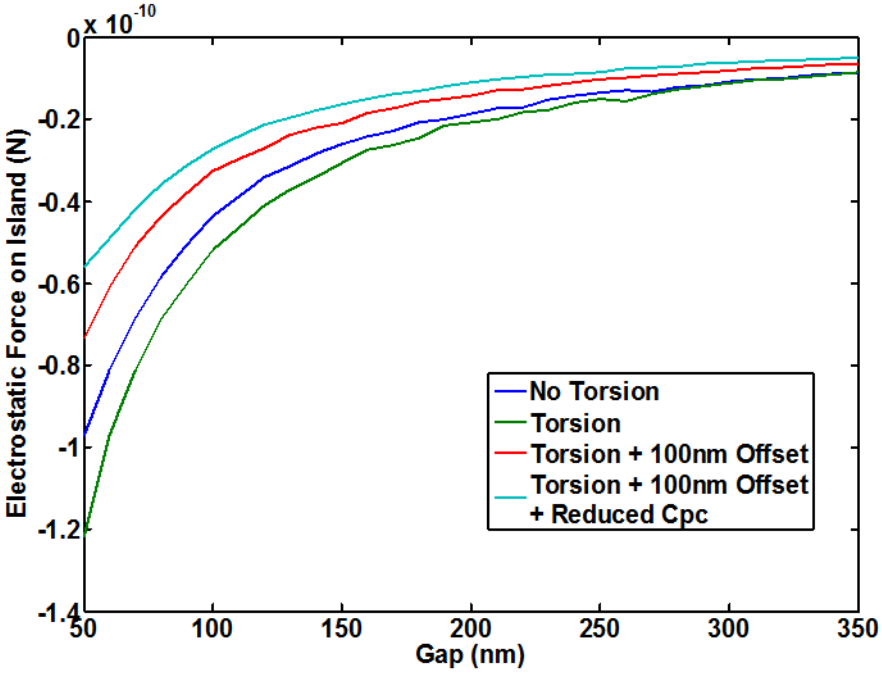


Figure 2.17: Electrostatic force curves for four different device configurations. Analysis describes the effects of practical designs on electrostatic force. 100 nm offset corresponds to Gate offset from Source/Drain. Reduced C_{PC} describes a device without A_{rel} (Section 3.5.3).

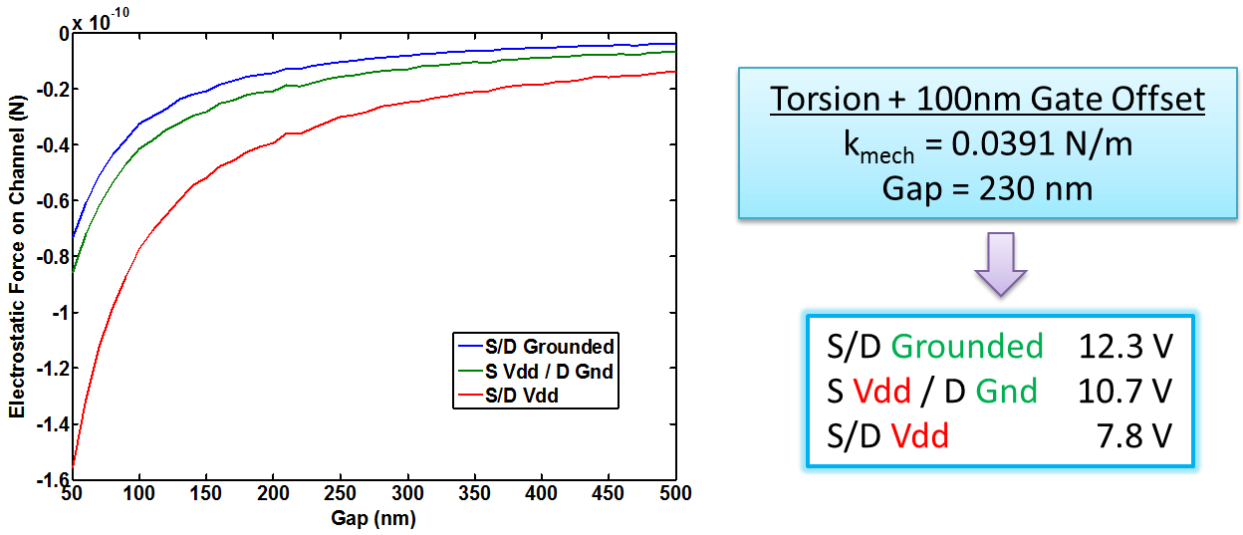


Figure 2.18: Electrostatic force curves for three different biasing conditions of Source and Drain. Curves are for two electrodes grounded, one electrode grounded, and both high. The figure summarizes the effects of Source/Drain bias on device operation voltage, as determined by the pull-in voltage.

FEM analysis was also used to ascertain the effect of the Source and Drain voltages on the overall operation voltage of the switch. The three most likely biasing conditions for the Source and Drain are 1) Source and Drain both grounded, 2) only one of the Source and Drain grounded, and the other electrode high, 3) both Source and Drain high. The three force curves were generated for a torsion-based structure with a 100 nm offset between the Gate and Source/Drain. Each curve was used to find the pull-in voltage under the given biasing conditions for a nano-pillar of typical dimensions. A $k_M = 0.039\ N/m$ corresponds to a pillar with non-uniform thickness, 130 nm at the bottom, and 180 nm at the top, with an approximate height of 10 µm. The initial gap size was 230 nm. Equation 2.11 was evaluated with the fitting parameters for the three curves in Figure 2.18 to yield the pull-in voltage for each biasing condition. When the Source and Drain are grounded, they contribute the least to the electrostatic

force on the Channel. However, when they are both high, there exists a larger voltage difference across a wider portion of the Channel, thereby increasing the electrostatic force on the Channel, and vastly decreasing the pull-in voltage of the device. Therefore, even the 4-terminal device is substantially influenced from the state of the Source and Drain.

2.6 PILLAR DESIGN

The design of the pillar depends primarily on the choice of the material system. Although this work focused on silicon-based devices, alternate material combinations can be potentially used.

2.6.1 Materials

Silicon's wide array of well-developed etching technologies, high quality intrinsic and deposited insulators, and beneficial electronic and mechanical properties, has kept it at the forefront of electronics. And for these same reasons, silicon has been the most widely used material for MEMS and NEMS systems. However, as opposed to planar devices, which generally use deposited thin films for the structural layer, a vertical device has its critical dimensions determined by lithography. This can be seen as a potential challenge for top-down vertical devices. Grown and deposited thin films enable tight control of thickness over large areas. Top-down vertical devices will require high aspect ratio etches with good selectivity to etch masks, to achieve the dimensions required for low voltage operation. Silicon is a natural choice given the BOSCH deep etch which can achieve aspect ratios up to 70:1 [71]. Additionally, the intended use will establish the requirements on speed and reliability. And one additional consideration will play a key role in material choices, process integration. If the nano-

relays will be incorporated with CMOS, will they be fabricated atop CMOS with low temperature processing, or can they be fabricated on a dedicated NEMS chip and stacked using 3-D technology? Clearly, if the nano-relays can be fabricated independently, the process latitude and materials choices can be greatly expanded.

Rather than restrict processing to less than 425 ˚C, pillar design will be discussed in the context of 3-D integration. Ideally the substrate material should be a conductor to enable the formation of a capacitive voltage divider, with the Channel – Pillar capacitance being one of the two capacitors. However, an insulator can be used if a conducting path can be formed on the exterior of the pillar. This thin layer would connect to another thin metallic layer under the Channel, thereby retaining an electrostatic configuration similar to the structure with a conducting substrate (Figure 2.19). In practice, sputtered or evaporated coatings for an insulating pillar would need to have very low residual stress, or be uniformly deposited on both sides of the pillar to prevent stress induced deflection or deformation. For insulators, silicon dioxide proves to be a good candidate for a pillar material. One approach is to start with a silicon deep etch and then used repeated oxidation and wet etching to thin the silicon pillar thickness. A final oxidation can then be used to oxidize the remaining silicon pillar. This method retains the benefits of deep silicon etching. A silicon oxide or quartz substrate can be used, with a substantial decrease in the aspect ratio [72]. Silicon dioxide has a Young's modulus ranging from 57 GPa for dry thermal oxide to 70 GPa for wet thermal oxide [73]. Single crystal silicon, by comparison, has a Young's modulus of 169 GPa in the <110> direction [62]. Materials with lower values for Young's modulus can lead to devices with lower operating voltage.

Another interesting option for a conducting substrate is Titanium. The Young's modulus of Titanium is 96 GPa ± 12 Gpa, and the tensile strength is approximately 0.95 ± 0.15 GPa [74]. Inductively coupled plasma etching of a bulk Titanium substrate has been shown to produce high aspect ratio pillars [75]. High tensile strength of some metals can make for robust structures with minimum concern of fracture and fatigue. Sputter deposited films have high residual stresses, from hundreds of MPa to over a GPa [76][77]. For a single-clamped cantilver/pillar, residual stress is not as problematic as it is for double-clamped beams. However, a stress gradient is more influential on a single-clamped structure, particularly for planar structures. An out-of-plane stress gradient in a deposited structural layer for a planar device will cause deflection of the mechanical element upon release. However, for a vertical structure, an out-of-plane stress gradient will not cause significant difficulties, as there is no net bending moment applied to the pillar. Therefore, metallic structures can be considered for future designs.

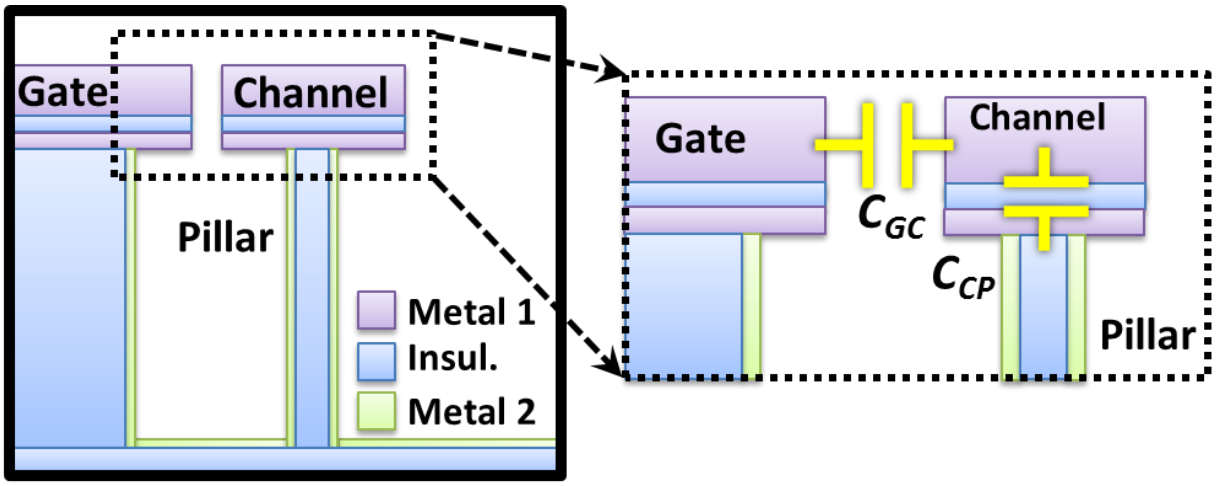


Figure 2.19: Top-down vertical structure that uses a pillar with an insulating core, and a conducting cladding to form a conduction path to the metallic layer underneath the Channel.

2.6.2 Scaling & Young's Modulus Size Effects

Starting with the simple expression for the stiffness of a pillar/ribbon with rectangular cross-section, we can discuss the scaling of the mechanical component of the device. The bending stiffness of a single-clamped beam is given by:

$$k_M = \frac{EW_{STEM}L_{STEM}^3}{4H_{STEM}^3} \tag{2.30}$$

The stiffness of the pillar has a cubic dependence on both thickness of the pillar, L_{STEM}, and the height, H_{STEM}. The height and thickness cannot be completely independently scaled. Due to finite aspect ratios of etching in top-down processes, consideration must be given to both of these parameters. Additionally, as pillar thicknesses scale below ~ 170 nm for silicon, the thickness begins to couple with the Young's modulus, *E*, of the material [78]. Li showed that single crystal silicon with thickness of 300 nm, and $E = 167\ GPa$, diminishes to $E = 53\ GPa$ for a 12 nm thick sample. Surface effects such as dangling bonds and surface relaxation cause deviation from the bulk behavior [79]. Initially, the thickness of the device, which is the smallest dimension of the structure, is first defined and limited by lithography. For a given stiffness, a combination of thickness and height can be chosen based on the etching technique. Thickness can also be difficult to scale for processes such as the BOSCH etch, where scalloping can lead to substantial variation of the pillar thickness for aggressively scaled devices. Recent etchers can achieve scalloping of less than 35 nm [80]. Although, even smoother results are possible, at the cost of selectivity to the etch mask. Ultimately, it may be beneficial to aggressively scale the electrostatics rather the mechanics. Decreasing pillar stiffness decreases the ability to the turn off the switch, and to reproducibly switch. The mechanical stiffness is needed to overcome the

Van der Waals forces present at the contact [11]. For applications that require one time programming, certainly a decrease in mechanical stiffness is acceptable.

2.7 SCALING & OPTIMIZATION

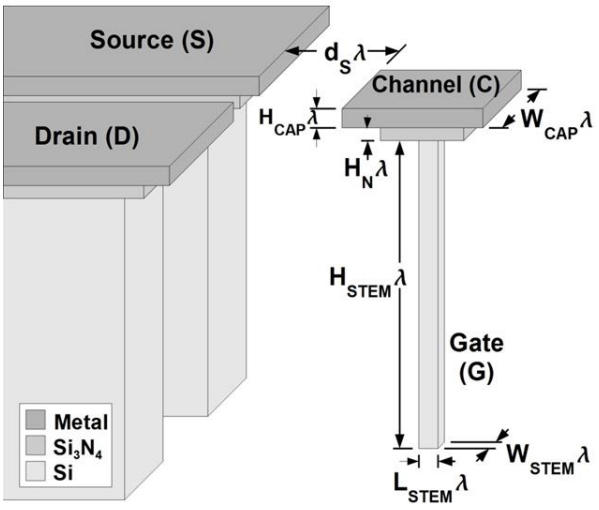
Scaling of a vertical top down nano-relay is explored using the pull-in voltage as the primary metric for device performance. More specifically, scaling is analyzed in terms of eight design parameters linked to device performance, and a general scaling parameter, λ, that accounts for uniform scaling of all dimensions as determined by the lithographic node. The analysis will discuss the practical tradeoffs of scaling individual parameters, and which parameters are most and least effective for improving device performance.

2.7.1 Parameter Space

The scaling analysis is performed using the three terminal device in Figure 2.20 as a basis. The three terminal structure enables use of the analytical model developed in Section 2.5.1. Although the four terminal device is more practical, scaling of the three terminal device helps us to gain intuition about the device operation and design. Additionally, the four terminal structure should follow similar scaling trends given that it is also based on a capacitive voltage divider, and follows the same general expression for electrostatic force derived in Section 2.5.1, as seen by the curve fitting of the FEM analysis in Section 2.5.4.

The scaling curves are generated by holding all parameters constant and only varying one parameter. The dimensionless parameter, λ, is used to vary all parameters simultaneously. It corresponds to the CMOS initiative of constant field scaling. The base point corresponds to a device that is close in size to our current devices, as outlined in Figure 2.20. The analysis also

assumes Si_3N_4 as the insulator, although high-κ dielectrics could be beneficial to device performance. Additionally, the pillar is assumed to have a uniform rectangular cross-section, thereby enabling the stiffness to be described by Equation 2.30. Young's modulus scaling is also including for a silicon pillar, as discussed in Section 2.6.1. Size effects of silicon primarily influence L_{STEM} and λ scaling. As with the previous analytical analysis, fringing fields are disregarded, and the Source, Drain, and Channel electrodes are assumed to have vertical sidewalls. A_{rel} is included. A base point value of 3 corresponds to a three times area increase of the capactive plate under the Channel over the cross-sectional area of the pillar.



(a)

Base Point (λ = 1)	
H_{STEM} λ = 9 µm	H_N λ = 100 nm
d_S λ = 200 nm	W_{CAP} λ = 2.35 µm
L_{STEM} λ = 150 nm	W_{STEM} λ = 1.75 µm
H_{CAP} λ = 500 nm	A_{rel} = 3

(b)

Figure 2.20: Schematic used for depicting the scaling parameters. (a) A three terminal device is used for ease of analysis. A_{rel} is not depicted. Its definition is consistent with Section 3.5.3. λ is the dimensionless scaling parameter. (b) The base point for the scaling plots corresponds to a device with the dimensions outlined in the chart.

The scaling curves in Figure 2.21 can be categorized in three ways. The scaling parameters depicted in the plot represent the least effective design components for scaling a structure given the starting base point.

Case 1: A_{rel} increase, or H_N decrease. Both changes cause the pillar/gate capacitance, C_G, to increase. With A_{rel} = 3 as the base point, we can see from Equation 2.2 that the potential of the floating Channel is initially $V_C = 0.83\ V_P$. Therefore, the potential is already pinned quite close to the applied Pillar/Gate voltage. Further increases in C_G bring the Channel potential closer to the Pillar potential. And electrostatic force increases as $V_C - V_S$ increases, in accordance with Equation 2.3. However, the change in pull-in voltage is not very substantial for further coupling of the Gate to the Channel.

Case 2: H_{CAP} increases, or W_{CAP} increases. Both changes cause the source capacitance, C_S, to increase. Therefore, $V_C - V_S$ decreases. Although the force per unit area is smaller, the area the force is applied is increased. Therefore, the net effect on electrostatic force is non-monotonic, in accordance with Equation 2.3. There exists and optimum size for these two parameters. However, a decrease in pull-in voltage may not be worth a substantial increase in the width of the device. The thickness of the metal electrodes can be increased with minimal detriment to device area. These parameters also have no effect on the mechanical properties of the structure.

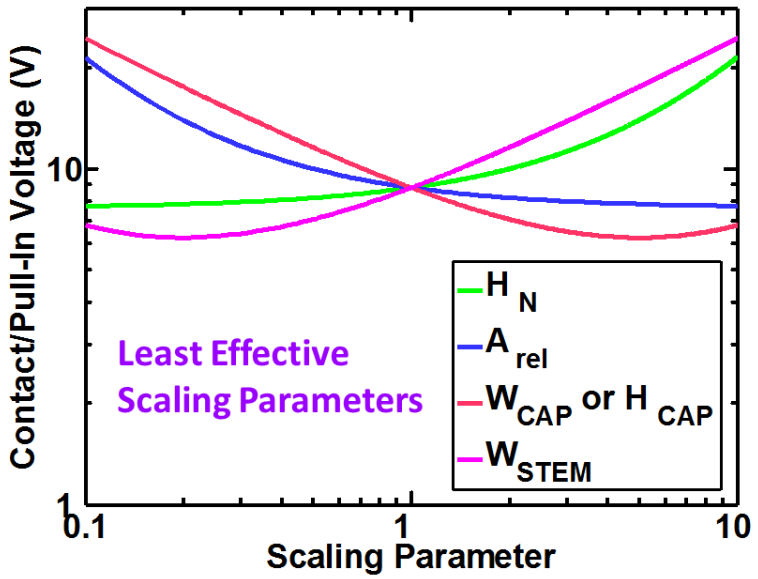


Figure 2.21: Scaling curves for the five least effective design parameters. W_{CAP} and H_{CAP} share a scaling curve, and have the same relationship to pull-in voltage scaling.

Case 3: W_{STEM} increases. The gate capacitance increases, thereby increasing $V_C - V_S$, and enhancing the electrostatic force. However, W_{STEM} also influences the mechanics of the device. Stiffness of the pillar increases, in accordance with Equation 3.30. Therefore, the scaling curve is non-monotonic. With a four terminal torsion-based device, it is possible to optimize the coupling of the pillar to the Channel and the stiffness of the pillar independently.

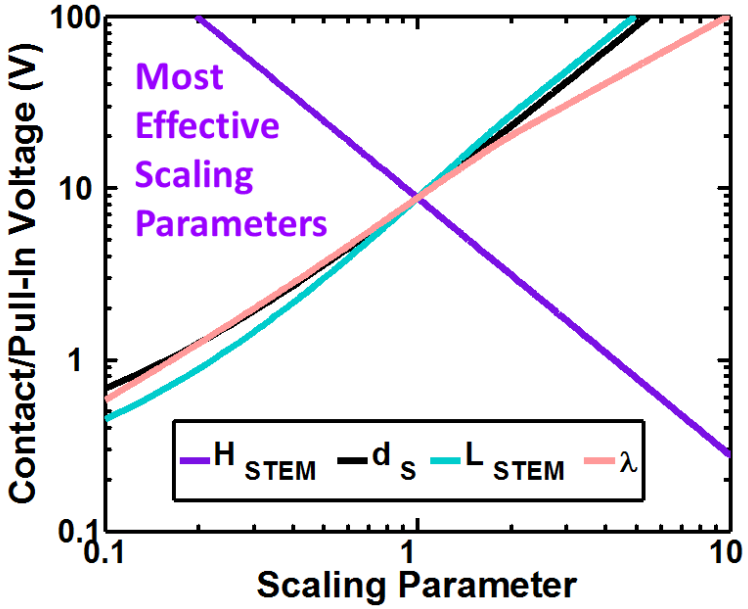


Figure 2.22: Scaling curves for three most effective design parameters. With λ scaling included for constant field scaling.

The scaling curves in Figure 2.22 can be categorized in four ways. The scaling parameters depicted in the plot represent the most effective design components for scaling a structure given the starting base point.

Case 1: H_{STEM} increases. This parameter only affects the mechanical properties of the device. Stiffness of the pillar decreases for increasing height. Although a tall pillar can bring the operation voltage down to below a volt, the aspect ratio required may not be physically

realizable. The base point corresponds to a pillar with a 60:1 aspect ratio. Additionally, decreasing the stiffness further reduces the ability of the device to overcome Van der Waals forces.

Case 2: d_S decreases. Decreasing the gap between the Source/Drain and the Channel does increase the source capacitance, thereby decreasing $V_C - V_S$. However, the more significant effect on the electrostatic force comes from the d_S^2 term in the denominator of Equation 2.3. Therefore, decreasing gap strongly decreases the operation voltage. And for practical devices with evaporated metallic electrodes, the gaps can be reduced without pushing the lithography. If electrodes with vertical sidewalls are desired, decreasing the lithographically defined gaps in the first step of fabrication will require a higher aspect ratio deep etch to achieve the desired pillar profile.

Case 3: L_{STEM} decreases. Decreasing the thickness of the pillar decreases the mechanical stiffness. The drawbacks are analogous to the case of H_{STEM}. Additionally, Young's modulus scaling has been included in the scaling curve. And as mentioned in Section 2.6.1, surface effects, damage, and etch non-uniformities will become more significant for thinner pillars.

Case 4: λ decreasing. Scaling all dimensions uniformly also achieves low voltage operation. Decreasing the device scale by a factor of 10 will result in a device with less than one volt operation. Additionally, λ scaling keeps the device within the bounds of conventional processing.

2.7.2 Fabrication Considerations

From the scaling analysis in Section 2.7.1, it is clear that in a top down vertical design the aspect ratio of the pillar is one of the most challenging design components. For bottom up

vertical designs [59][81] high aspects ratios are quite easy to achieve. Planar devices use thin film processes and lithography to carefully control the aspect ratio of the mechanical element. Therefore, a vertical top down device requires careful control of the height and thickness to guarantee operation at voltages comparable to planar devices. A number of methods have been devised for achieved high aspect ratio pillars.

2.7.2.1 Oxidation & Wet Etching

The most straightforward approach to making high aspect ratio pillars without pushing the limits of deep etching requires a modest deep etch with aspect ratio ~ 30:1, and subsequent thinning of the pillar. One well established method for thinning silicon is thermal oxidation and wet etching. Oxidation of silicon, as described by the Deal-Grove model, results in tightly controlled thicknesses of both silicon and the resulting oxide. Using this method, it is quite simple to start with a pillar with 0.5 μm thickness and reduce it to a final thickness of 100 nm. Wet processing can be challenging for high aspect ratio structures. Therefore, repeated oxidations and HF wet etches must be handled with care when the pillar thickness and the Source/Drain to Channel gap become small, thereby producing conditions that are conducive to stiction. After removing the silicon dioxide with HF/BOE, the wafer is rinsed in deionized water. Stiction results during drying, when capillary forces due to the surface tension of the water between the Channel and the Source/Drain and Gate cause the Channel to adhere to the Source and Drain. Stiction during wet processing is generally considered irreversible for delicate nano-scale structures [82]. Therefore, stiction is avoided by using critical point drying to circumvent the liquid phase during drying. Figure 2.23 illustrates the oxidation and wet etching process in stages. Additionally, Figure 2.24 demonstrates the powerful potential of this approach

for producing extremely high aspect ratio, uniform nanoribbons and nanopillars. The nanoribbon shown there has a thickness of ~ 55 nm, and an aspect ratio greater than 140:1. The oxidation process also has the added benefit of reducing the sidewall roughness from the characteristic scalloping of the BOSCH process.

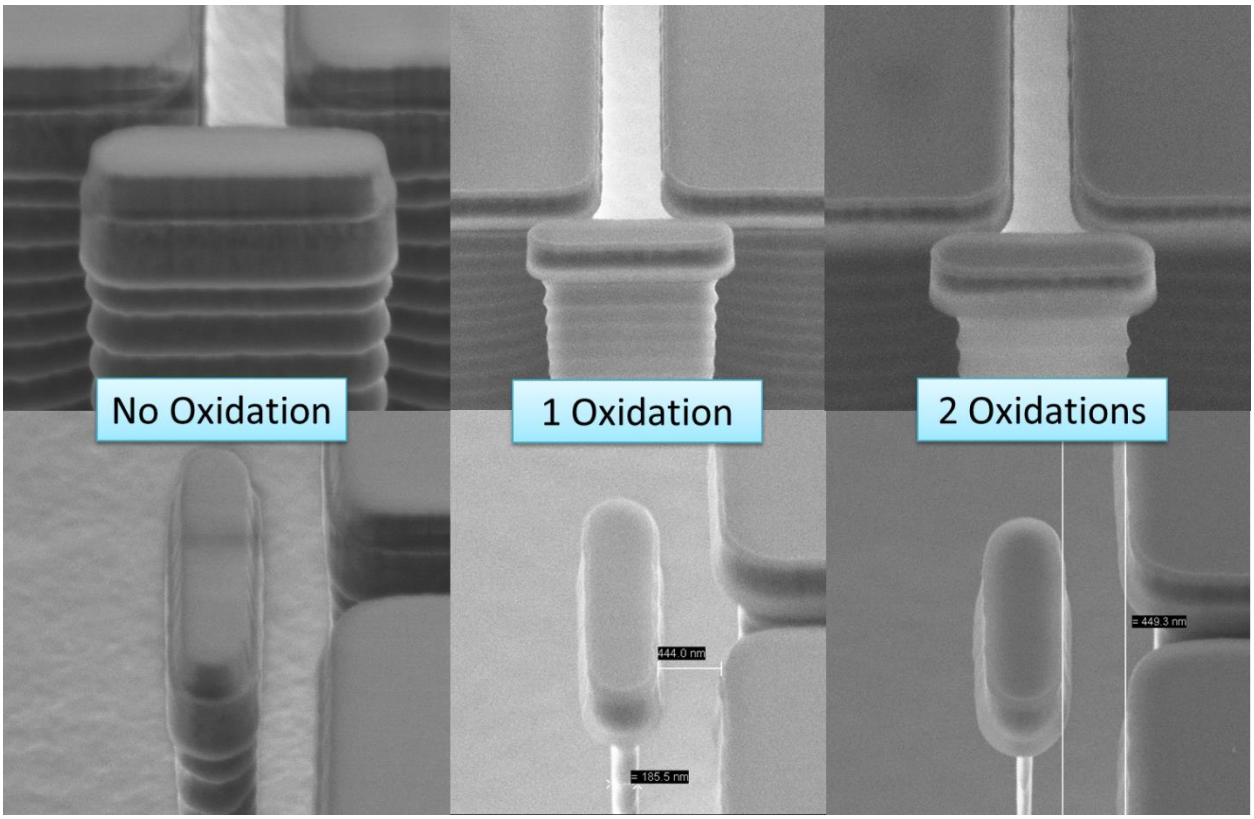


Figure 2.23: SEM images of three terminal device. (a) Front and side view of pillar before oxidation. Scalloping from BOSCH deep etching process is readily apparent. (b) After one oxidation and wet etch removal of silicon dioxide. (c) After two oxidations and removal of silicon dioxide. Substantial reduction in ribbon thickness is noticeable.

One of the main disadvantages of this approach is that high temperature processing is required to achieve a significant amount of size reduction using oxidation. If vertical nanorelays are to be incorporated directly atop silicon transistors, low temperature processing will be required. A similar approach is possible using plasma-assisted oxidation [83]. The resulting

silicon dioxide has similar electrical and chemical properties to thermal oxide. Film thickness uniformity can also be somewhat challenging with this approach.

The most significant challenge to the oxidation method is a negative effect similar to the bird's beak that occurs with local oxidation in CMOS [84]. Silicon oxide growth under the silicon nitride diffusion barrier results in expansion and permanent deformation of the silicon nitride. Figure 2.23 shows a structure with a vertical silicon nitride sidewall, used to protect the underlying silicon, for implementation of the A_{rel} method for voltage reduction in Section 2.5.3. During successive oxidations, the bottom lip of the nitride sidewall undergoes plastic deformation. Figure 2.23 shows the sidewall expansion at the bottom of the feature, thereby resulting in a bell-like structure. Figure 2.25 shows a cross-section of a pad where the silicon has undergone oxidation beneath the nitride sidewall. After removing the silicon dioxide, deformation of the sidewall is readily apparent.

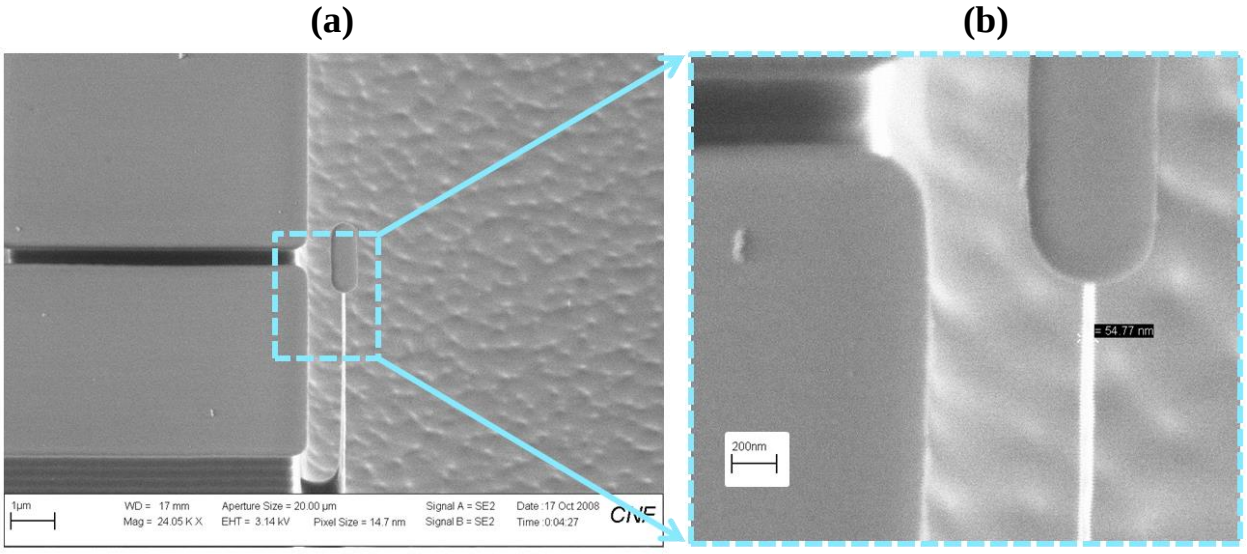


Figure 2.24: SEM images of high aspect ratio three terminal device. (a) Aerial view of structure. Image shows extremely high aspect ratio nanoribbon, and demonstrates the uniformity of thickness possible with this approach. (b) Enlarged view of the nanoribbon structure. Image shows a nanoribbon with a thickness of ~ 55 nm. The nanoribbon is attached to a silicon nitride island that serves as a diffusion barrier for oxidation, an electrical insulator, and a structural support for the metallic Channel.

The final step of fabrication is to perform a blanket metal evaporation. This forms the electrodes and the Channel simultaneously. The metallization also determines the final gap size, d_S, and the height of the variable capacitor, H_{CAP}. Generally a few hundred nanometers of metal are required for a device similar to those shown in Figure 2.23. Metal should ideally deposit only on the planar silicon nitride layer for a device with vertical sidewalls, given a directional deposition process. However, Figure 2.26 (a) shows metal deposition on the top silicon nitride, but also a band of metal around the bottom lip of the sidewall. The device in Figure 2.26 (b) without a sidewall shows a cleaner metal profile, with deposition only on the top surface. Figure 2.27 illustrates the difficulty with the oxidation method, and the ensuing sidewall profile. If the bottom lip of the sidewall protrudes beyond the top edge, a directional evaporation will deposit metal in both locations. This continues throughout the deposition. Ultimately, the bottom lip will remain extended beyond the Channel on top. During operation, contact will be made between adjacent bands/protrusions of metal, instead of the Channel contacting the Source/Drain electrodes. The metal is discontinuous between the top electrodes and the band at the sidewall lip, separated by a vertical region of silicon nitride. Therefore, no Source/Drain current is measurable during operation.

A simple solution could be to use an angled evaporation, thereby depositing metal on the entire sidewall. However, for a device with a narrow Channel and a high aspect ratio pillar, much of the pillar stands to be exposed to metal deposition as well. This raises difficulties with thin film stresses and increasing overall thickness of the pillar. Additionally, utilizing deformation of the sidewall will not result in well-defined gap sizes. A better solution will be to find a method of size reduction that leaves the sidewall with a vertical profile. It should be noted that for devices without sidewalls, the oxidation method still has many advantages. Furthermore,

self-limiting oxidation enables ultimate scalability for vertical nanopillars. For pillars with initial diameters of less than 50 nm, sub-5nm diameters silicon pillars can be consistently achieved [85]. Self-limiting oxidation results in tightly controlled pillar thicknesses as a result of stress induced reduction of oxidation. Additionally, HF vapor can be used for highly scaled devices, whereby wet processing can be avoided entirely. Therefore, oxidation is a very useful method of size reduction for silicon-based devices.

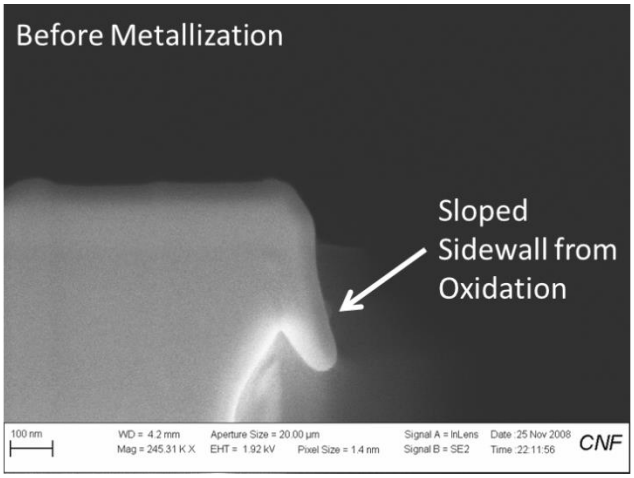


Figure 2.25: SEM image of cross-sectioned pad on device employing silicon nitride sidewall process for A_{rel} voltage reduction. Image shows sidewall deformation from local oxidation.

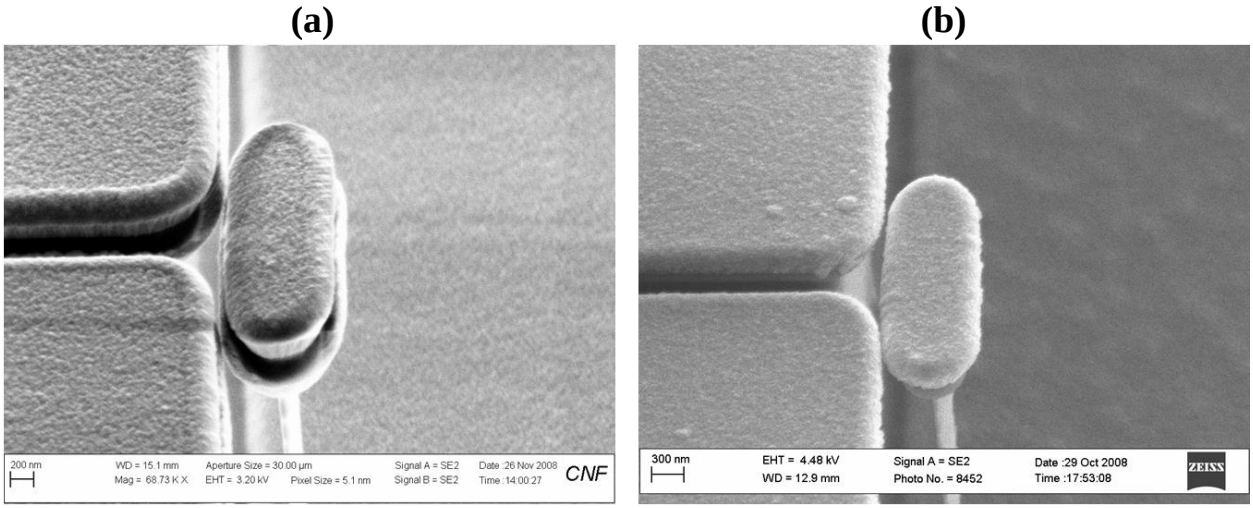


Figure 2.26: SEM images of completed three terminal devices with metallization. (a) Device with silicon nitride sidewall. Metal evaporation occurs simultaneously on bottom of sidewall lip and planar top silicon nitride layer. (b) Device without silicon nitride sidewall. Metal evaporation only deposits on top silicon nitride layer to form Channel.

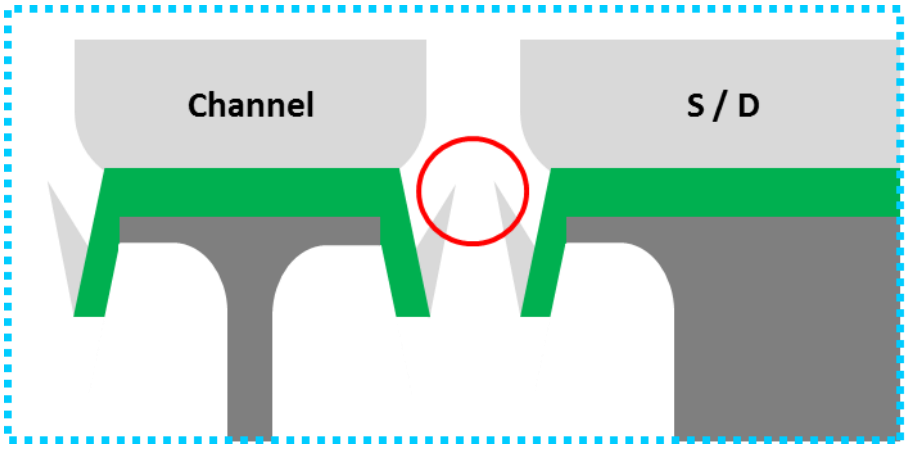
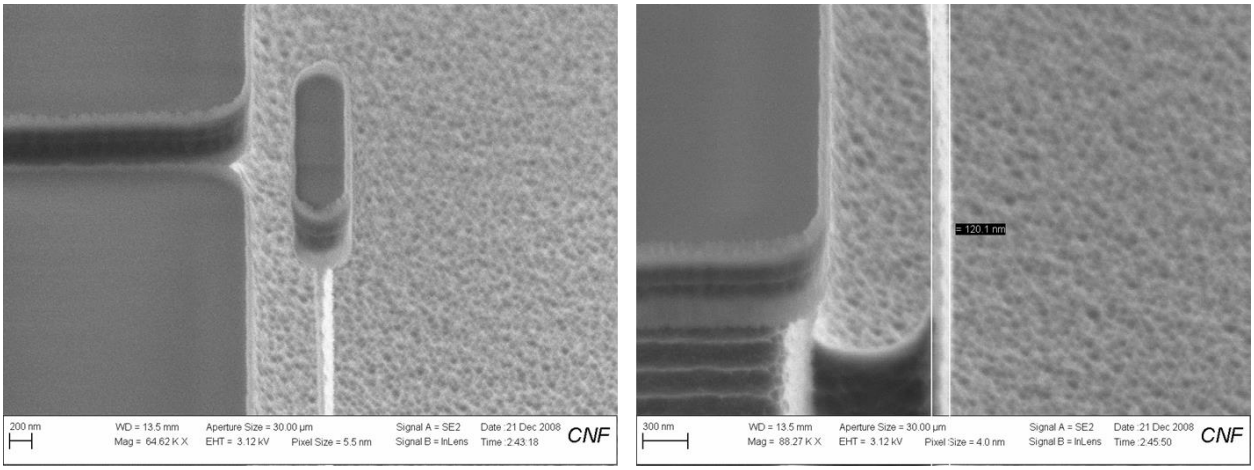


Figure 2.27: Schematic of structure with silicon nitride sidewall and deformation of sidewall due local oxidation. Side view shows metal evaporation at bottom of lip. During operation, device makes contact between metal protrusions at bottom of lip. No current is measured since metal protrusions are electrically isolated from metal electrodes on top of the planar silicon nitride.

2.7.2.2 HNA Etch & Critical Point Drying

Another solution to achieving high aspect ratio devices is to use isotropic silicon wet etching. A combination of HF/Nitric/Acetic acid (HNA) can be used to produce an isotropic silicon etch. Nitric acid oxidizes the silicon surface and HF dissolves the silicon dioxide. The acetic acid is a diluent and prevents excessive dissociation of the HNO_3 [86]. Although silicon oxide etches in HNA, silicon nitride is conveniently a good etch mask. For a similar silicon etchant solution (126 HNO_3 : 60 H_2O : 5 NH_4F) at room temperature, the etch rate of silicon is 150 nm/min, with a selectivity of 750:1 to silicon nitride [87]. Generally isotropic wet etching is reserved for non-critical tasks with large geometries. And etch rates of HNA can typically be from a few microns per minute to tens of microns per minute [86]. Therefore, etch rate and roughness are not particularly easy to control with HNA. A low etch rate is necessary for the small size scale of the current device. Etch rate did fluctuate with usage and stirring time.

Figure 2.28 (a) shows a device with vertical sidewalls after HNA etch. Slight roughening of the silicon nitride is noticeable. Figure 2.28 (b) shows a high aspect ratio nanoribbon achieved with the isotropic silicon etch, where the ribbon thickness is ~ 120 nm. Some pitting and roughness is noticeable, as is characteristic of HNA. However, this recipe produced fairly smooth surfaces; in accordance with recent work [88]. Since this size reduction method requires wet processing, critical point drying is absolutely necessary to avoid stiction. Figure 2.29 shows a cross-section of a pad, where silicon etchant has undercut the silicon nitride sidewall. The sidewall appears nearly vertical, and silicon is maintained beneath the planar nitride for A_{rel} implementation. Finally, metallization is performed, and no deposition of metal occurs on the sidewall, as seen in Figure 2.30. The SEM image shows a device making contact at the top of the metallic Channel after pull-in. This experiment demonstrates the ability to make high aspect ratio top down vertical structures without extensive high temperature processing. However, controlling the ribbon/pillar thickness is extremely challenging using this method. A similar method in the gaseous phase would be to use XeF_2 to reduce the silicon. Although wet processing could be avoided, critical dimension control would be equally difficult with XeF_2, as high etch rates of ~ 0.5 – 3 μm/min are quite typical [87]. When nitride deformation is avoided, the desired metal profile is achieved. Therefore, another approach must be found that gives tighter control of critical dimensions, while still avoiding sidewall deformation and extensive high temperature processing.



(a) **(b)**

Figure 2.28: SEM images of three terminal devices fabricated using poly-etch to reduce the ribbon thickness. (a) Thinned vertical structure. Undercut of silicon clearly visible by charging in the SEM. (b) Nano-ribbon with uniform thickness of ~ 120 nm. Image shows roughness and pitting of the silicon, characteristic of poly-etch.

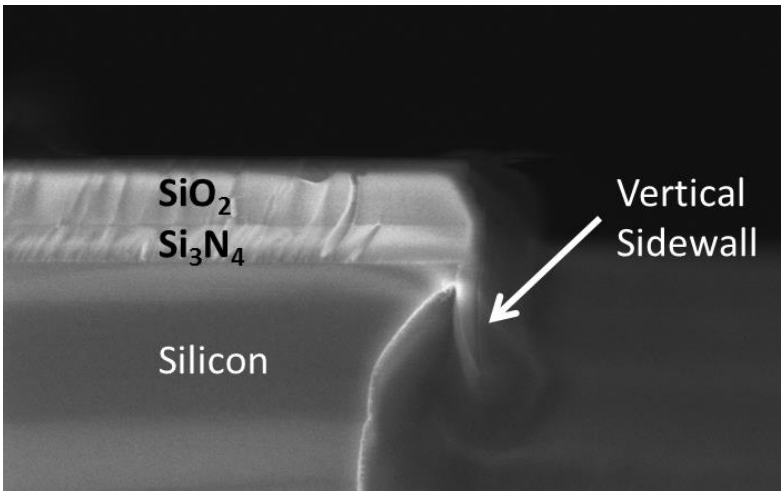


Figure 2.29: SEM image of cross-sectioned pad on device employing nitride sidewall. Silicon thinning performed using poly-etch. Image shows that silicon is retained at the junction of the planar and sidewall nitride. Also, nitride sidewall appears more vertical than the oxidation method of size reduction.

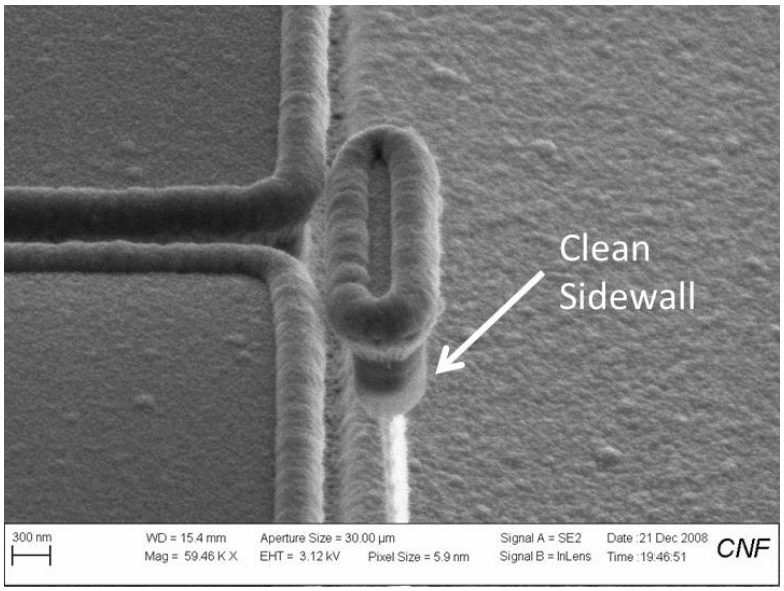


Figure 2.30: SEM image of completed three terminal device with metallization. Image shows no deposition of metal on the nitride sidewall. Contrast of the bottom lip of the sidewall arises from charging of the silicon nitride in the SEM, where silicon has been removed by the poly-etch.

2.7.2.3 Plasma Etch Size Reduction

One additional approach to isotropic silicon removal is SF_6/O_2 reactive ion etching. A baseline process with pressure of 20 mTorr, 25 sccm SF_6, 10 sccm O_2, and an RF power of 100 W can result in a silicon etch rate of ~ 1500 nm/min in a parallel plate reactor such as the STS 320 [87]. In order to etch ~ 200 – 300 nm/min of silicon from either side of the structure, the etch rate had to be slowed significantly to enable repeatable and controllable etching. A modified process was initially used with pressure of 15 mTorr, 30 sccm SF_6, 6 sccm O_2, and an RF power of 30 W to achieve an etch rate of ~ 100 nm/min. Furthermore, SF_6/O_2 is not particularly selective to Si_3N_4, whereby a selectivity of 10:1 is seen with the parameters quoted for the STS 320 above [87]. However, the etch we performed showed significant etch rate

dependence on silicon nitride orientation. Although the top planar nitride etched slightly, the sidewalls remained relatively untouched. Figure 2.31 shows a four terminal device with high aspect ratio pillar formed using the dry isotropic silicon etch. The silicon nitride sidewall remained intact during the etching. This may be due to the importance of ion bombardment for silicon nitride etching in fluorine chemistry [89]. Ion bombardment of a vertical sidewall in a parallel plate reactor with SF_6/O_2 chemistry may not be sufficient to induce isotropic etching of silicon nitride. This enabled nitride thickness to stay relatively constant in all three size reduction schemes mentioned in Section 2.7.2. Additionally, the silicon surface is relatively smooth, thereby enabling substantial reduction in critical dimensions. A noticeable non-uniformity in pillar width and thickness is present. The pillar profile is tuned by both the BOSCH deep etch and the silicon isotropic dry etch. Using dry etching to achieve uniform silicon nano-pillars will be further discussed in Chapter 5. Figure 2.32 shows a device after metallization. The sidewalls appears vertical and clear from metal deposition. Using this method we obtained the first functional top down vertical four terminal devices. Although the devices were exposed to a plasma, charging did not result in premature pull-in during processing. Figure 2.33 shows an SEM of a cross-sectioned pad after metallization. The silicon nitride sidewall is nearly vertical, with no significant metal deposition on the bottom lip. Additionally, the silicon undercut is minimal beneath the nitride sidewall. This may be a result of reduced ion bombardment by nitride shielding. A shorter sidewall could be employed if the silicon etch is not perfectly isotropic, as less silicon needs to be protected to employ A_{rel} improvement. Although thickness control of the pillar with plasma etching is not as predictable as the oxidation method, it is the method we employed most since it eliminates the sidewall deformation issue, reduces process time, and requires no wet processing.

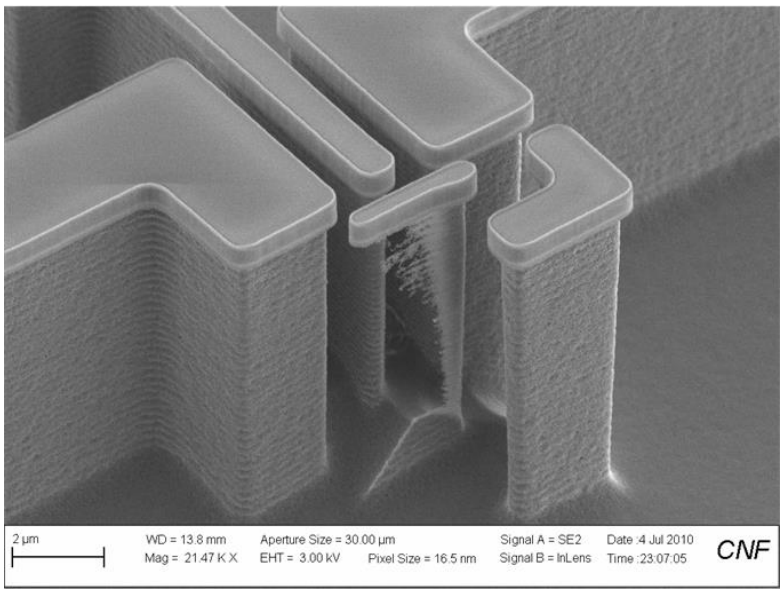
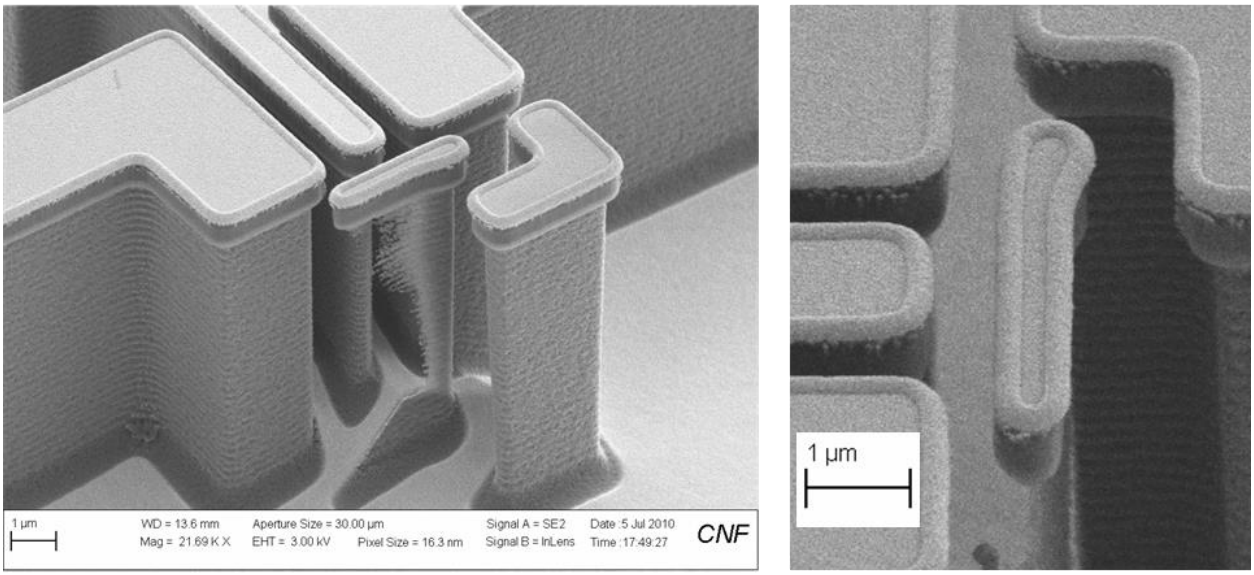


Figure 2.31: SEM image of four terminal device fabricated using isotropic dry etching with SF_6/O_2. Pillar profile depends on both initial deep etch profile and isotropic SF_6/O_2 parameters.



(a) **(b)**

Figure 2.32: SEM images of four terminal device after metallization. (a) Metal evaporation appears only on the top planar silicon nitride layer. (b) Side view of device shows verticality of sidewalls.

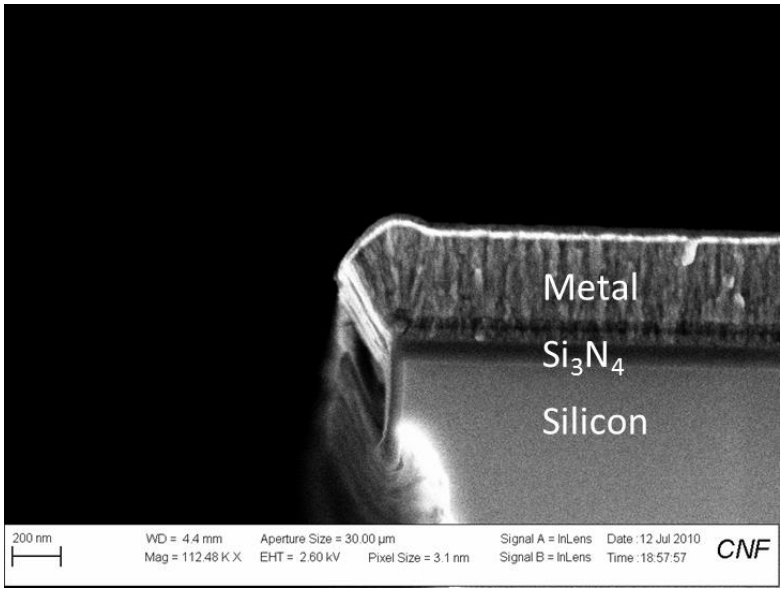


Figure 2.33: SEM of cross-sectioned pad after metallization. Metal stack is Ti/Al/Ti/Au from bottom to top. Silicon nitride sidewall remains quite vertical and clear from deposited metal. Undercut of silicon beneath sidewall minimal.

CHAPTER 3

DESIGN/FABRICATION OF THREE TERMINAL NEMS SWITCH

3.1 OVERVIEW

Building on the previous chapter, this chapter will discuss the fabrication process, and device characteristics of a three terminal NEMS switch. Device characteristics will be explored using an optical measurement known as the knife-edge method. Additionally, the simple analytical model for a three terminal device will be extended to non-contact pull-in voltage extraction. Using the knife-edge method in combination with the analytical model, the pull-in voltage is determined for a number of devices. The optical measurement is also used to calculate the Young's modulus for an array of devices with different silicon ribbon thicknesses. Analysis of the fabricated three terminal devices will lead to sensible designs for the four terminal devices.

3.2 THREE TERMINAL FABRICATION PROCESS

The three terminal devices require very simple mask design and produces silicon nano-ribbons of uniform thickness. The fabrication procedure uses only a single step of optical lithography, with all subsequent processing self-aligned. By patterning the Channel, Source, and Drain all in one lithography, alignment of the Channel to the Source/Drain electrodes is limited only by line edge roughness and other non-uniformities introduced by subsequent processing. Initial devices were fabricated using i-line lithography, with a minimum feature size of 0.65 μm. However, such a substantial gap size would result in devices that require a high voltage exceeding 20 V. Therefore, a liftoff process was chosen for pattern transfer to enable over-

exposure of the gaps, d_S, thereby reducing one of the critical dimensions. While over-exposing the gap, the Channel length, L_{CAP}, increases in size a proportional amount to the gap reduction. Increasing L_{CAP} increases the operation voltage. Therefore, silicon thickness reduction is used to increase the aspect ratio of the device. An initial Channel that is larger can simply undergo further size reduction. This enables over-exposure to be useful for improving device operation.

Fabrication begins with ⟨100⟩ silicon wafers, N++ (0.001 Ω•cm), single-side polished. Heavily doped wafers are used in accordance with the discussion in Section 3.3.1, where consideration was given to the effects of charge depletion. Next, 150 nm of LPCVD stoichiometric Si_3N_4 is deposited on a MOS cleaned silicon surface. Although standard nitride is highly stressed, it is chosen as the platform and insulator for the electrodes and Channel owing its low leakage current, resistivity to buffered oxide etch, and ability to serve as a diffusion barrier for thermal oxidation of silicon. PECVD SiO_2 is deposited atop the nitride. It defines the maximum height of the Si_3N_4 sidewall for A_{rel} implementation, and as a hard etch mask for the BOSCH deep etch. The oxide thickness must be chosen such that the surrounding nitride sidewall does not etch back below the planar nitride layer during the silicon deep etch, step 5 in Figure 3.1. The etch rate of Si_3N_4 compared to SiO_2 in a BOSCH process is approximately 3:1 (process dependent) [90]. And the selectivity of unannealed PECVD SiO_2 to silicon is ~ 150:1 – 200:1, with an etch rate of silicon of ~ 1500 – 2400 nm/min [91]. Therefore, to achieve 10 μm nano-ribbons, a minimum of 50 nm of PECVD oxide is needed for the etch, thereby requiring at least 150 nm of Si_3N_4. To have a nitride sidewall of at least 150 nm, there needs to be at least the same about of oxide to form the sidewall. We deposited ~ 430 nm of undoped PECVD oxide at 400 ˚C. This thickness allows room for poorer selectivities, and over-etch in the sidewall etchback step (step 4 in Figure 3.1).

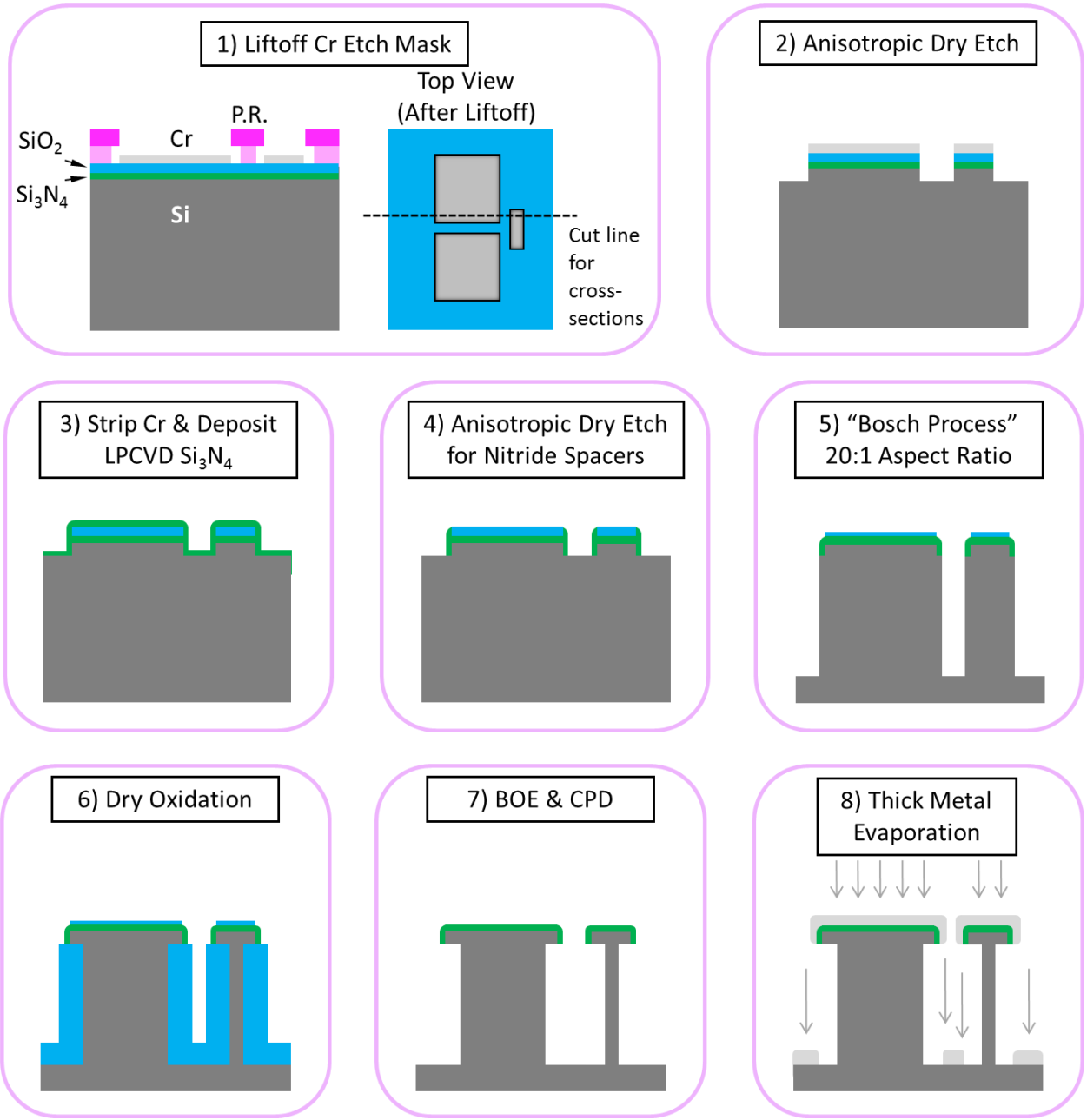


Figure 3.1: Schematic of fabrication procedure for three terminal top-down vertical device. Cross-section of device shows Channel and adjacent electrode. (1) Liftoff Cr etch mask using bilayer resist process and overexposure to reduce gap size. (2) Shallow anisotropic dry etch through $SiO_2/Si_3N_4/Si$ stack. (3) Remove Cr etch mask with dry and wet processing. Deposit LPCVD Si_3N_4 to encapsulate silicon substrate with conformal nitride. Nitride sidewall protects silicon for A_{rel} implementation. (4) Anisotropic dry etch to form nitride sidewall spacers. (5) Silicon deep etch for defining initial ribbon dimensions. (6) Oxidation of nano-ribbons to reduce dimensions. (7) Buffered oxide etch to remove SiO_2, and critical point drying to avoid stiction. (8) Metallization with directional deposition. Forms electrodes and reduces gap size further.

A bilayer resist process is used to perform the liftoff process. A process consisting of Shipley LOR 3A and Oir 620-7i was optimized for the feature size. Controlling the undercut of the liftoff resist was extremely critical. With too much undercut, narrow features in the top layer of resist become suspended, thereby leading to sagging and stiction issues during development and rinsing. Additionally, chrome deposition can migrate under suspended features, and cause unwanted deformation of the resist from high thin film stress. The chrome deposition was accomplished by thermal evaporation. For deposition rates much greater than ~ 0.3 Å/s and thicknesses greater than ~ 60 nm, the high tensile residual stress in chrome caused cracking in regions of suspended resist. In-plane stress measurements of chrome thin films have yielded values as high as 1.27 – 1.45 GPa on a Si_3N_4 substrate [92]. Similar values of stressed chrome on top of photoresist can cause significant damage. Cracking leads to stringers of chrome on the substrate beneath the fracture. And the selectivity of a chrome etch mask to the $SiO_2/Si_3N_4/Si$ stack in fluorine chemistry is significantly high, such that a few nanometers of chrome on the substrate will pattern transfer.

After completing liftoff of ~ 35 nm of thermally evaporated chrome, an RIE process in a parallel plate reactor with CF_4 chemistry is used to transfer the pattern into the $SiO_2/Si_3N_4/Si$ stack. The etch parameters are 150 W RF power, 40 mTorr chamber pressure, and 40 sccm CF_4. Etching ~ 33 minutes achieved a step height of ~ 940 nm. This height includes ~ 325 nm etched into the silicon substrate, as seen in Figure 3.2. The silicon must be etched to a depth such that later thinning of the silicon nano-ribbon does not fully remove the silicon under the Channel for A_{rel} implementation. Figure 3.3 shows the requirements for silicon depth. The isotropy of the thinning method will determine the exact depth of the silicon. For nano-ribbons with an initial thickness of ~ 600 nm, and a desired final thickness of ~ 100 nm, a silicon depth of at least ~ 250

is required. The depth should actually exceed this to allow for there to be a significant silicon layer under the planar nitride layer. Before depositing the LPCVD Si_3N_4 sidewall in a CMOS furnace, the chrome etch mask must be removed. An RIE etch with Cl_2 + O_2 chemistry is used to strip the chrome. Additionally, wet chrome etch consisting of $22\%\ (NH_4)_2Ce(NO_3)_6 + 8\%\ CH_3COOH + H_2O$ [93] by Cyantek is used to complete the etch at room temperature. Then a MOS clean is performed, and ~ 90 nm of conformal Si_3N_4 is deposited. The interface between the planar nitride and the nitride sidewall must be clean to prevent any unwanted leakage paths from the substrate to the electrodes and Channel.

Step 4 in Figure 3.1 entails an anisotropic dry etch to etch back the conformal nitride. Care must be taken to ensure that the nitride is completely removed in the small gaps between the Channel and the Source/Drain. 7 minutes of RIE was used in a parallel plate reactor with CHF_3/O_2 chemistry to clear the nitride on the substrate and define the nitride sidewall. Figure 3.4 shows the nitride sidewall. The nitride appears to be over-etched, with the top of the sidewall recessed below the PECVD oxide. Additionally, the Channel has a footing at the bottom of the feature. Close to the vertical sidewall, the footing may be nitride. This is a result of heavy polymerization on the nitride sidewall, thereby inhibiting the etch at the bottom of the feature. The polymer was removed using oxygen plasma. Etching of the nitride was interspersed with short one minute oxygen plasma etches to keep the polymer buildup from obstructing the nitride on the substrate. Following the nitride etch-back is the silicon deep etch. Any remaining nitride on the surface around the features will be cleared during the deep etch from ion bombardment.

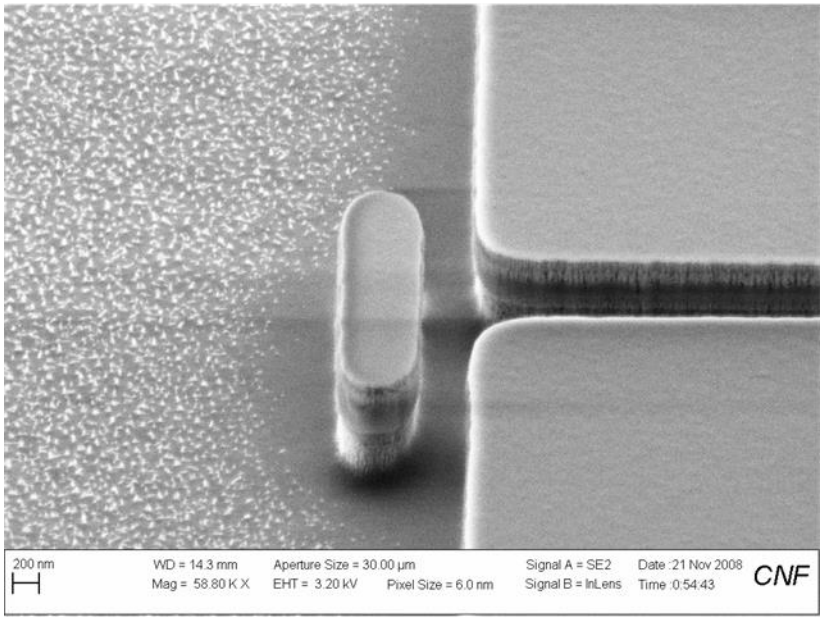


Figure 3.2: SEM image of second fabrication step in Figure 3.1. Chrome etch mask still intact on top surface. Contrast between SiO_2 and Si quite pronounced. Silicon appears slightly recessed under the oxide/nitride.

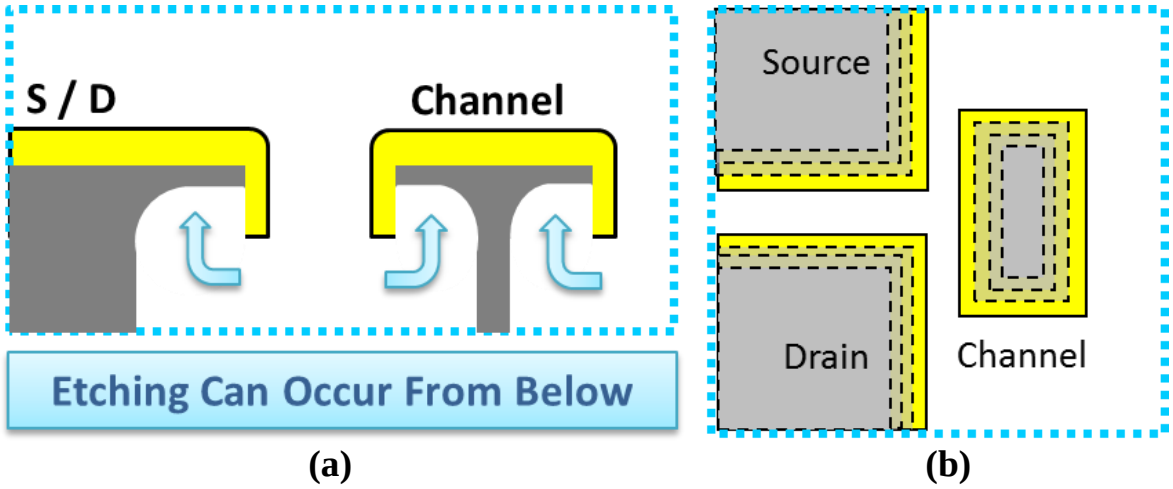


Figure 3.3: Depending on the size reduction method (oxidation, silicon wet etching, plasma etching, etc.), varying degrees of undercut will occur. (a) Removal of silicon behind Si_3N_4 sidewall decreases the thickness of the silicon electrode underneath the Channel. (b) Schematic of silicon removal process. Silicon removal effects both length of ribbon, L_{STEM}, and width of ribbon, W_{STEM}.

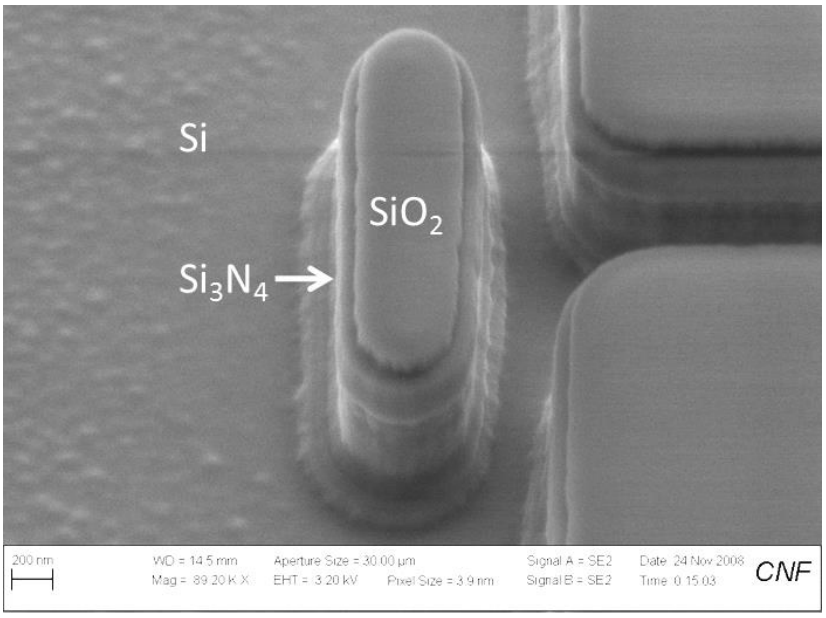
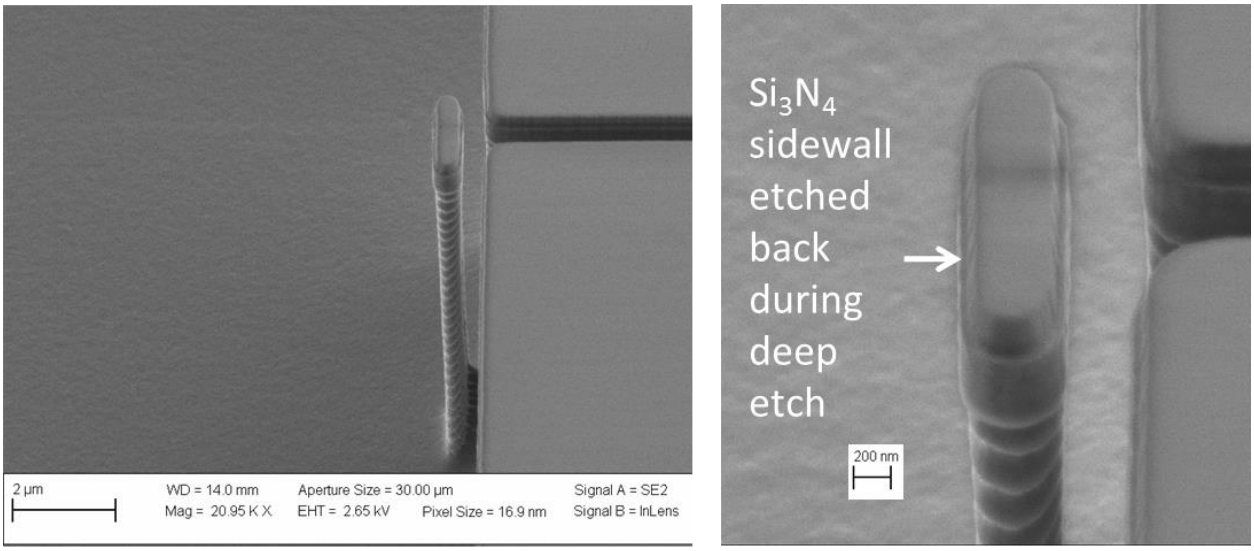


Figure 3.4: SEM image of structure after fourth fabrication step in Figure 3.1. Silicon nitride sidewall clearly encircles the oxide etch mask. The silicon nitride has been etched slightly below the level of the oxide. Footing on bottom of features is silicon (and possibly a thin Si_3N_4), which was protected during the anisotropic etch-back of the Si_3N_4 due to polymerization on the silicon nitride sidewall.

The BOSCH etch uses an inductively coupled plasma (ICP) to produce a dense plasma. RIE in a parallel plate reactor has a plasma density of ~ 1 – 5 x 10^9 / cm^3 [94], whereas ICP can have a density of ~ 5 x 10^{11} / cm^3 [95]. Additionally, the ion energy is controlled by a separate RF source, thereby enabled high density plasmas with low ion energies for high selectivity and etch rates. The BOSCH process cycles between C_4F_8 and SF_6 chemistry. The C_4F_8 is used as a passivation gas, whereby all surfaces are coated with a C_xF_y thin flouro-carbon polymer film. Ion bombardment during the SF_6 etch serves to preferentially break through the passivation layer on the substrate due to the directional nature of a capacitively coupled plasma in a parallel plate configuration [96]. For the etch we used, the etch rate was ~ 300 nm/cycle. The rate is pattern dependent. 27 cycles were run for a total step height of ~ 9 µm at the center of the wafer, including the height of the film stack and silicon within the nitride sidewall, as seen in Figure

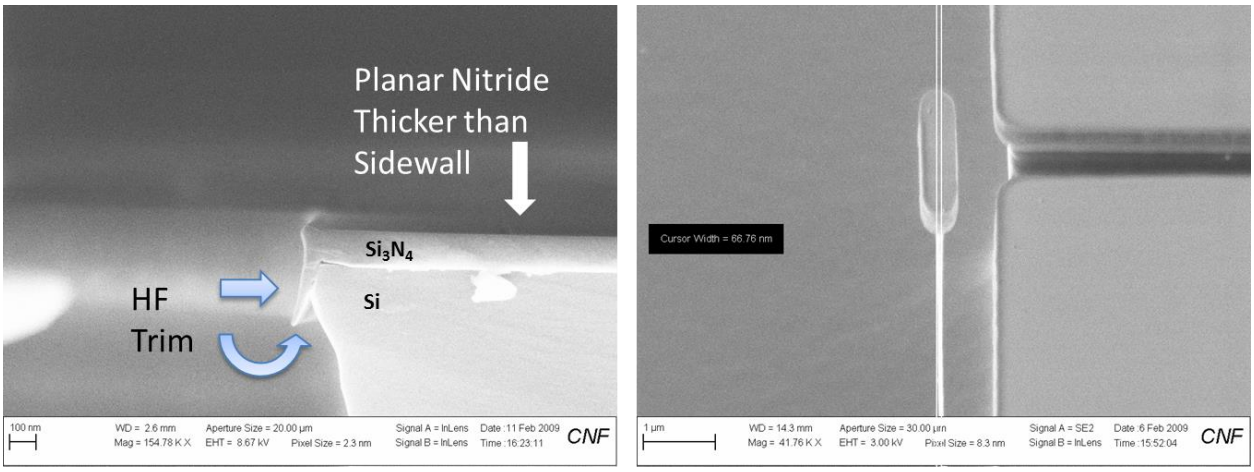
3.5(a). Also, the nitride sidewall etched faster than the PECVD oxide, but remained intact around the encapsulated silicon, as seen in Figure 3.5(b). Scalloping of the silicon is accentuated in this etch. With process step times for passivation and etching in the range of seconds, scalloping can be noticeable. As step times decrease to sub-second range, scalloping improves.

The next step is to increase the aspect ratio of the nano-ribbon. In Section 2.7.2 we discussed the various techniques for size reduction in silicon. The first method we employed was the oxidation and wet etch approach in Section 2.7.2.1. The desired thickness was achieved using three successive dry oxidations. The oxidations were performed at 1100 ˚C to attain a substantial oxidation rate. The oxidation was broken up in order to lessen the deformation of the nitride sidewall. Following each oxidation, the oxide was removed with BOE 6:1. The sample was then transferred to methanol after being rinsed in DI H_2O. Critical point drying was used to avoid stiction. Figure 3.6 (a) shows a problem with the protruding nitride lip, as we discussed in Section 2.7.2.1. With three oxidations the nitride lip is less pronounced than with two. However, it still posed difficulties during metallization. One potential solution is to dip the sample in HF 49% solution after the device has the desired dimensions. LPCVD stoichiometric Si_3N_4 etches at ~ 14 nm/min in HF 49%. This slow etch can be used to trim the protruding lip and any remaining nitride sidewall above the planar nitride. The corners etch faster in the solution since they are exposed on both sides of the film, as depicted in Figure 3.6 (a). Critical point drying must once again follow this step. The result can be seen in Figure 3.6 (b) for 5 minutes in HF. The pronounced sidewall deformation seen post-oxidation is no longer present. The nano-ribbon shown there has an impressive thickness of ~ 65 – 70 nm.



(a) **(b)**

Figure 3.5: SEM image of structure after fifth fabrication step in Figure 3.1. (a) Trench on right side of nano-ribbon starts to pinch off at the bottom. Trench and nano-ribbon have an aspect ratio of ~ 20:1. (b) Comparing the nitride sidewall in this figure to Figure 3.4, Si_3N_4 seen to etch faster than silicon dioxide, with nitride sidewall almost level with planar nitride.



(a) **(b)**

Figure 3.6: SEM of device after size reduction and nitride lip removal. (a) Cross-section of pad after two oxidations and BOE etches. Nitride lip protrudes beyond the top of the feature. HF can be used to trim nitride and smooth sharp corners. (b) High aspect ratio structure after HF trim and critical point drying. Nano-ribbon thickness is ~ 65 – 70 nm.

The final step in Figure 3.1 is metallization of the device. The metallization forms the Source/Drain electrodes and the floating Channel. Additionally, the top substrate contact is formed for measurement purposes. E-beam evaporation was used for directional deposition. Approximately 30 nm of titanium was deposited, then ~ 50 nm of aluminum at ~ 1 Å/s, another 300 nm of titanium was deposited at ~ 3 Å/s, followed by ~ 60 nm of gold at ~ 1 Å/s. Gold was used for initial testing to eliminate the possibility of oxidation at the contacts, and for easy wire bonding to the devices. In Figure 2.33, and Figure 3.7, thick deposition of metal can be seen to lead to shrinking of the gap size. Metal deposits at the edge of the feature and builds up beyond the edge. This effect is advantageous for low voltage switches which require small gaps.

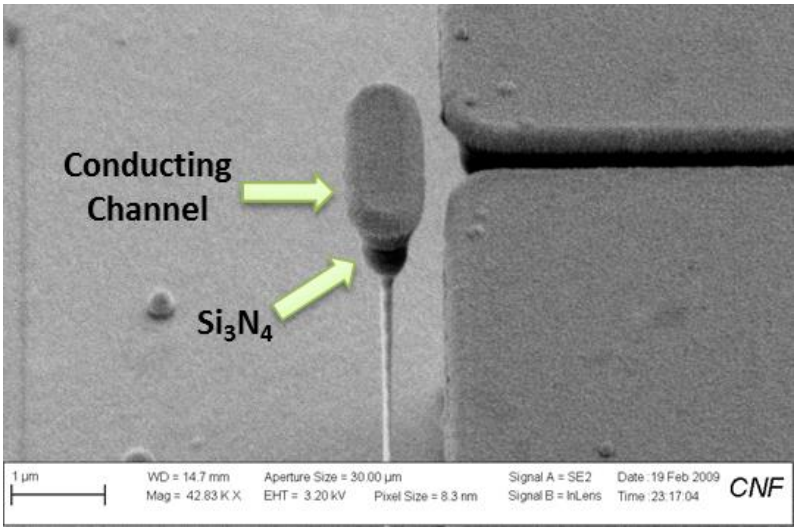


Figure 3.7: SEM image of device with metallization. Nitride sidewall appears quite clean using HF trim to smoothen sharp features.

3.3 DEVICE CHARACTERISTICS

Initial measurement of the three terminal devices was performed using an optical measurement technique developed by the Craighead Lab at Cornell University, as shown in Figure 3.8. Dynamic characterization of the nano-ribbon can be achieved by optical excitation

and detection. The setup uses electro-optic modulation of a blue diode laser (415 nm) to cause local temperature gradients in close proximity to the device. Temperature gradients give rise to stresses which couple mechanical energy to the device [97]. An additional HeNe laser (632 nm) with focused spot size of ~ 3 μm is positioned on the tip of the nano-ribbon/Channel. Variations from the incident laser caused by transduction of the device are detected by a single-cell photodetector. The measurement demonstrated that a small area device, with Channel size ~ 2 μm x 1 μm could be detected using this approach. Additionally, the method proved effective for measuring in-plane vibrations.

The preliminary results shown in Figure 3.9 helped us to realize that measurement in vacuum is quite essential for these devices. The device measured had an air gap, d_S, of ~ 260 nm, nano-ribbon thickness ~ 160 nm, height ~ 9 μm, and a resonant frequency of ~ 815 kHz. Low quality factors of ~ 40 at atmosphere were ascertained for this three terminal device. Detection is difficult for such low values of Q, and was only possible in the case where the precise resonant frequency was found initially with high vacuum. Once resonance is detected the pressure can be increased to observe the change in quality factor. At a pressure of ~ 1Torr, improvement in the quality factor levels off at a value of ~ 900. Other observed devices showed a similar trend. Therefore, to avoid air (viscous) damping, rough vacuum can provide substantial benefit. However, acoustic anchor losses, thermoelastic damping from bending stress gradients, and internal losses will still be present.

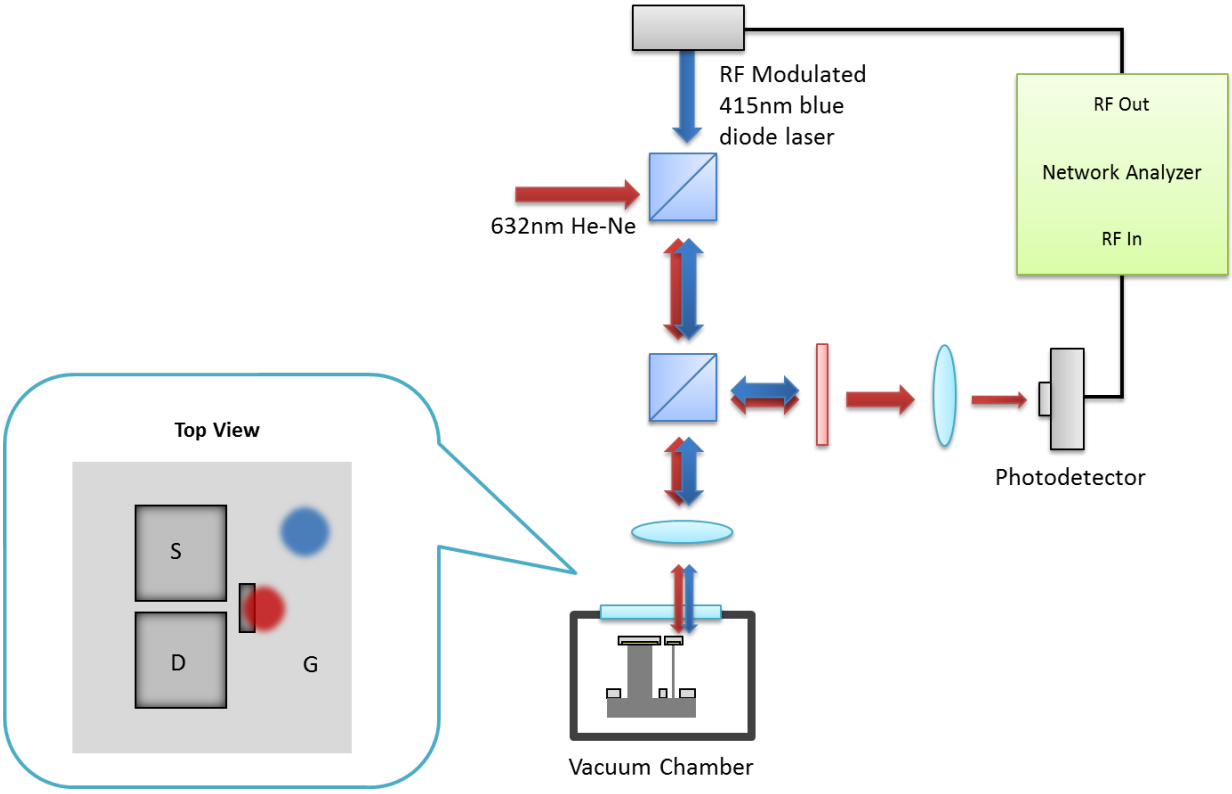


Figure 3.8: All-optical measurement setup for frequency measurement of micro- and nano-oscillators. Optical excitation and optical measurement of device using two lasers of different wavelength. Initial measurement performed in Craighead Lab in Cornell University.

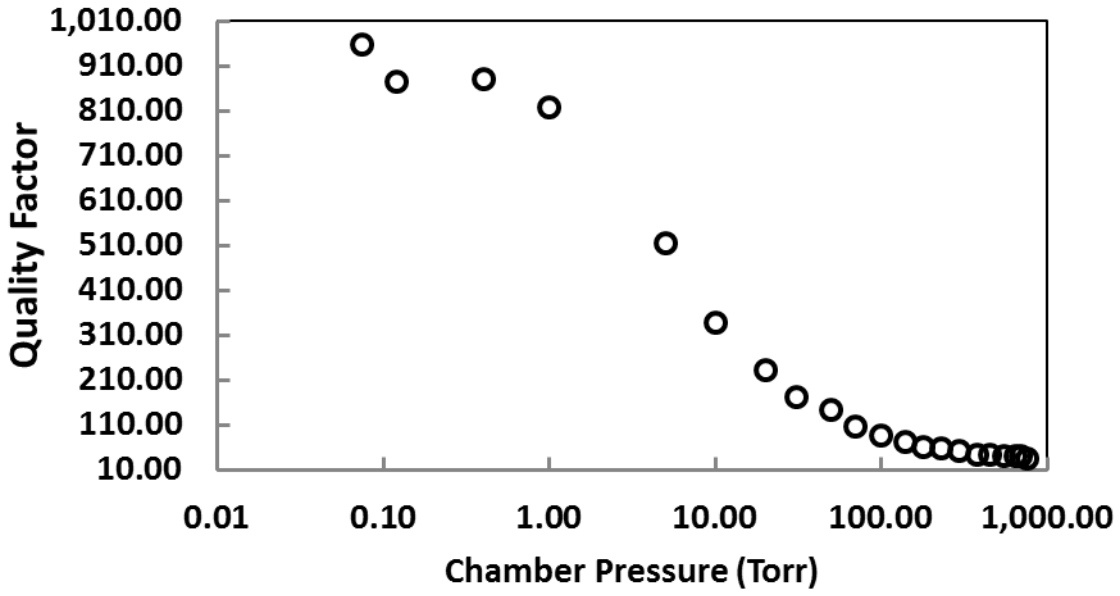


Figure 3.9: Quality factor of three terminal device fabricated with oxidation size reduction. Nano-ribbon height ~ 9 µm, and thickness ~ 160 nm.

Based on the success of the optical measurement technique, further characterization of the devices was performed with a similar setup we constructed for electrical excitation and optical detection, as seen in Figure 3.10. A custom vacuum chamber was constructed to enable easy recognition of the resonant peaks of the devices. A single HeNe laser was required for detection. The principle operation mechanism of sensing is understood to be the knife-edge technique [98]. Interferometry is particularly useful for devices that move out-of-plane, where optical path length change gives rise to intensity changes from constructive and destructive interference [99]. The knife-edge method is advantageous for in-plane actuation, where movement is perpendicular to the optical axis of the incident light. A diffraction limited laser spot is focused on the edge of the feature that is moving, in this case the Channel. When the device moves, the reflected light from the incident laser is modulated. A change in intensity occurs as the portion of the device in the path of the laser varies.

The sensitivity of the measurement depends on the difference in reflection between the moving feature and the substrate, and the difference in height between the top of the moving feature and the substrate, as depicted in Figure 3.11. As the device moves further into the path of laser, the substrate will contribute less to the overall reflection. If the top surface is more reflective than the substrate, the overall intensity of the reflected light will increase. The greater the contrast in reflectance between the device and the substrate the higher the sensitivity of the measurement system. The ideal case is a highly reflective device suspended over a void, i.e. no substrate [100]. The second condition for sensitivity is a result of using focused light. A perfectly collimated beam would not see a change in reflection from a moving structure suspended up a surface with identical reflectivity. However, with the beam focused on the top surface of the structure, greater defocus of the laser for larger height differences between the top

surface and the substrate can result in larger intensity modulation. For electrical excitation, our measurement system has a 24 pin DIP socket integrated in the chamber wall, with the socket leads used as feed through for the measurement. Therefore, many devices can be simultaneously bonded and measured without breaking vacuum. The HeNe laser is focused using a 50X Mitutoyo infinity corrected long working distance objective with numerical aperture of 0.55 for an optimal diffraction limited spot size of ~ 1 μm. For our particular devices, since metallization is a blanket evaporation, both the moving structure and the substrate are coated in identical films, thereby decreasing contrast. However, the 10 μm height of the nano-ribbons enables the measurement to be feasible.

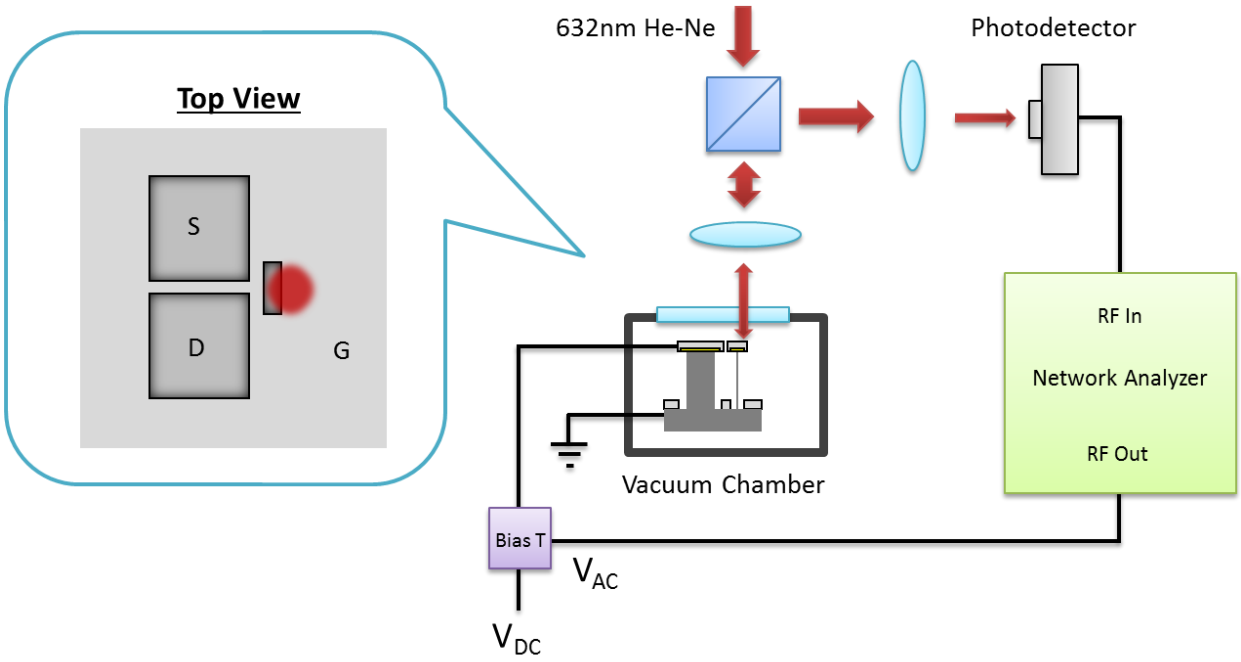


Figure 3.10: Measurement system for electrical input with optical output. System was built to accommodate 24-pin dip package for measuring many wire-bonded devices without modifying connections. Setup is useful for determining electrical coupling of devices and also their mechanical properties.

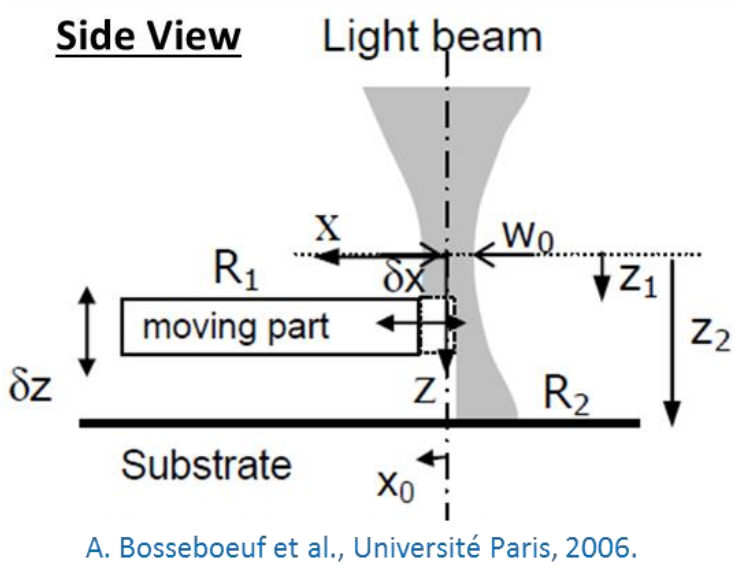


Figure 3.11: Knife-edge measurement technique. Schematic of relevant geometrical parameters for optical resolution, as determined by A. Bosseboeuf et al. [98]. Measurement requires either reflection difference (R_1/R_2) or height difference (Z_1/Z_2) between moving part and substrate.

Although this measurement technique can be used to find the resonant frequency of the device, thereby giving access to the mechanical properties of the structure, the measurement can also yield information regarding the pull-in voltage of the device without actual pull-in. An applied DC voltage on the Source/Drain of the device results in a corresponding shift towards lower resonant frequencies, a phenomena known as the negative spring effect or spring softening [5]. Therefore, a relationship can be established between applied voltage and the resonance frequency, thereby giving access to the electrical characteristics of the device. We use this approach to extract the pull-in voltages of the devices in a completely unobtrusive way, where contact can be avoided and stiction and other damaging interactions can be circumvented.

The derivation for the resonant frequency shift as a function of applied voltage starts by revisiting the expression we found in Section 2.5.1 for the electrostatic force on the Channel as a function of position:

$$F_E(x) \approx \frac{C_0 V_G^2}{2(d_0 + d_S - x)^2} \tag{3.1}$$

We can use a Taylor expansion to look at the electrostatic force for small motions near $x = 0$. This results in the Taylor series:

$$F_E(x) \approx \frac{C_0 V_G^2}{2(d_0 + d_S)^2} + \frac{C_0 V_G^2}{(d_0 + d_S)^3} x + \frac{C_0 V_G^2}{2(d_0 + d_S)^4} x^2 \tag{3.2}$$

The second term in the Taylor series has the form of a force due to a spring, with C_0, d_0, and d_S all constant. Therefore, the term is proportional to x, and has a spring constant (electrical spring constant) given by:

$$k_{el} = \frac{C_0 V_G^2}{(d_0 + d_S)^3} \tag{3.3}$$

Therefore, we can write an effective spring constant for the device as:

$$k_{eff} = k_M - \left.\frac{dF_E}{dx}\right|_{x=0} = k_M - \frac{C_0 V_G^2}{(d_0 + d_S)^3} \tag{3.4}$$

As the applied voltage increases, the electrical spring constant increases, thereby decreasing the effective spring constant for the structure. The electrostatic force causes an attractive force on the Channel, which detracts from the restoring effect of the mechanical spring constant. The overall decreases in the effective spring constant results in a shift towards lower resonant frequencies for increasing gate voltage. Next we perform a little algebra to write the expression in terms of frequency, the variable we will measure. Dividing Equation 3.4 by k_M and using the relationship $\omega = \sqrt{k/m}$, we arrive at the expression:

$$\frac{\omega_{eff}}{\omega_0} = \sqrt{1 - \frac{C_0 V_G^2}{k_M (d_0 + d_S)^3}} \tag{3.5}$$

Performing another Taylor expansion gives:

$$\frac{\omega_{eff}}{\omega_0} = 1 - \frac{1}{2}\frac{C_0 V_G^2}{k_M (d_0 + d_S)^3} \tag{3.6}$$

And rewriting this expression in terms of the change in resonant frequency:

$$\frac{\Delta\omega}{\omega_0} = -\frac{1}{2}\frac{C_0 V_G^2}{k_M (d_0 + d_S)^3} \tag{3.7}$$

We can now compare this equation to Equation 3.11, rewritten as follows:

$$V_{Pull}^2 \approx \frac{4}{27}\frac{2(d_0 + d_S)^3 k_M}{C_0} \tag{3.8}$$

This enables us to write an expression for resonant frequency shift in terms of the pull-in voltage of the devices. Pull-in voltage can then be extracted from measurements of frequency for different applied voltages. The final expression for resonant frequency shift for $V_G \ll V_{Pull}$ is given by:

$$\frac{\Delta\omega}{\omega_0} \approx -\frac{4}{27}\left(\frac{V_G}{V_{Pull}}\right)^2 \tag{3.9}$$

This expression can now be used to find the pull-in voltages for a number of devices using the optical measurement system with electrical excitation.

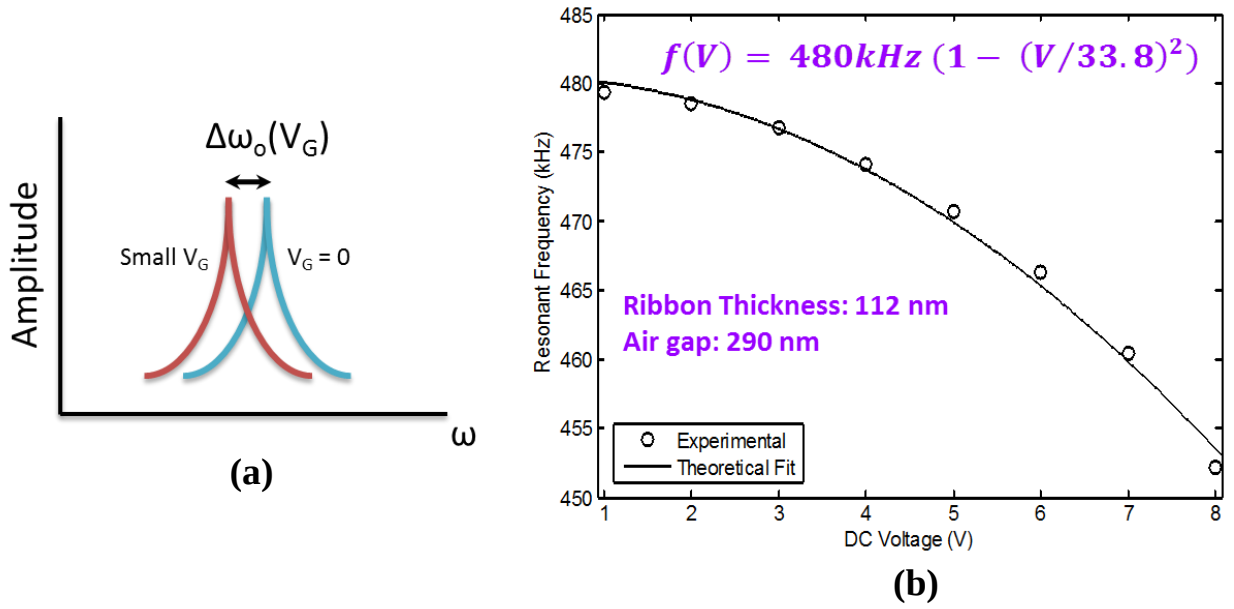


Figure 3.12: Pull-in voltage extraction of device from resonant frequency shift. (a) Schematic illustrating method and expected outcome for increasing gate voltage. (b) Resonance shift for applied voltages ranging from 1 to 8 volts with a theoretical fit in the form of Equation 3.6.

Figure 3.12 (a) shows the intended approach to pull-in voltage extraction. A small gate voltage should cause a corresponding shift in the resonance peak to lower frequencies, in accordance with Equation 3.9. Figure 3.12 (b) is plot of the actual experimental date for a device with nano-ribbon thickness of ~ 112 nm, and air gap of ~ 290 nm. The date is fit using a form of Equation 3.6 with two fitting parameters, the resonant frequency without a bias voltage and the pull-in voltage. The expression in Figure 3.12 (b) can be rewritten in the format of Equation 3.9:

$$\frac{\Delta\omega}{\omega_0} = -\left(\frac{V_G}{33.8}\right)^2 = -\frac{4}{27}\left(\frac{V_G}{13.0}\right)^2 \tag{3.10}$$

Therefore, the pull-in voltage for this particular device can be estimated at 13 V based on the quadratic fit of the experimental data. An additional benefit of this approach is that it is possible to estimate pull-in voltage even in devices that would not yield conclusive results in a DC sweep. For instance, a device with substantial line edge roughness or any other undesirable effect that gives rise to an offset between the Source and Drain, can be measured using this non-contact

approach. A DC measurement of Source/Drain current for gate voltages swept from 0 V up to and exceeding the pull-in voltage would pull-in the device without any significant signature of pull-in behavior. Simultaneous contact of the Channel to the Source and Drain is a necessary condition for DC measurement. Figure 3.13 shows a sampling of the measured devices using the non-contact method of pull-in voltage extraction. Devices with the lowest frequencies, i.e. lowest stiffness, and smallest gaps, i.e. highest electrostatic forces, have the smallest pull-in voltages. A device with an extremely small thickness of ~ 87 nm and gap of ~ 248 nm shows a pull-in voltage of less than 10 volts.

Thickness	Gap	Resonant Freq.	Pull-in Voltage
160	336	949250	41.1
152	287	889500	32.1
166	250	1089270	27.1
132	260	714800	24.1
115	331	492500	21.5
87	248	346000	9.2
112	290	480500	13.0
129	198	664500	14.6
120	296	572500	17.2
200	194	1524200	38.9
193	259	1395200	46.4

Figure 3.13: Summary of nano-ribbon devices tested using non-contact resonant frequency shift pull-in voltage extraction method. Thicknesses and gap sizes are in nanometers.

In addition to the shift in in resonant frequency, we can look at the absolute value for the resonant frequency to extract other pertinent features of the mechanics. Other work has used single and double clamped micro- and nano-beams to extract the Young's modulus of a material from the resonant frequency [78][101]. For cantilevers suspended over air gaps, careful

characterization of dimensions and simple structural geometries can enable accurate evaluation of the mechanical properties of the cantilever. Optical and electrical methods can be used to determine the resonant frequencies. And thin film deposition or growth techniques can be used to precisely control film thickness and uniformity. Although the geometry in our devices is slightly more complicated, material properties can be evaluated and measured in a similar fashion. Analysis of our particular structure can elucidate whether size effects are significant for the device and give further direction for future designs.

The general expression for the resonant frequency of a mass-spring model is given by $\omega = \sqrt{k/m}$. However, this expression is for a lumped system with a concentrated load mass positioned at the end of a massless spring. Our device does not resemble such a case. The load mass, Channel, can be less massive than the nano-ribbon depending on the metals used, and their respective thicknesses. Gold has a much higher density than silicon, thereby contributing significantly to the Channel mass and helping simplify the analysis to a point load. However, to extract useful information about the mechanical properties, a thorough analysis of the resonant frequency should be performed, with consideration given to the contribution of mass from the pillar. The standard expression for a lumped system was used previously in the derivation for Equation 3.9 since the effect of the modification is cancelled by looking for resonant frequency shift, rather than the absolute value of the resonant frequency.

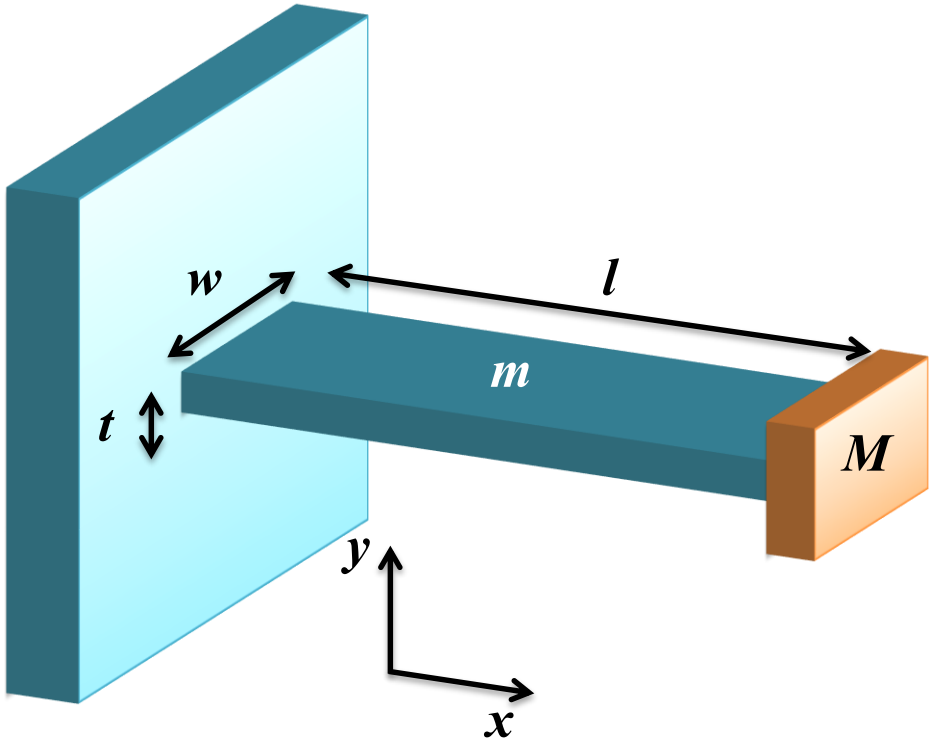


Figure 3.14: Schematic for cantilever resonant frequency analysis. Single clamped beam with beam mass, *m*, and load mass, *M*.

We begin the derivation by considering a cantilever beam along the x-axis clamped rigidly at x = 0, as shown in Figure 3.14. The beam will have density ρ, Young's modulus *E*, and a cross-sectional area defined as *w x t*, where *t* is the dimension in the bending plane. The area moment of inertia for such beam is $I = wt^3/12$. We will let a load of mass *M*, representing the mass of the Channel, be attached to the tip of the beam at beam at $x = l$. If we let the deflection of the neutral axis of the beam be described by $y(x,t)$, then the equation of motion for forced transverse vibrations can be described by the Euler-Bernoulli equation [102]:

$$\frac{\partial^2}{\partial x^2}\left(EI\frac{\partial^2 y}{\partial x^2}\right) + \rho A\frac{\partial^2 y}{\partial t^2} = f(x,t) \tag{3.11}$$

This governing equation is for an undamped beam. For our nano-ribbon structure we can assume a beam with uniform cross-sectional area and material properties. We can then look at the free vibration case, with $f(x,t) = 0$. Equation 3.11 simplifies to:

$$EI\frac{\partial^4 y}{\partial x^4} + \rho wt\frac{\partial^2 y}{\partial t^2} = 0 \tag{3.12}$$

This can be written more succinctly as:

$$\frac{1}{c^2}\frac{\partial^4 y}{\partial x^4} + \frac{\partial^2 y}{\partial t^2} = 0 \tag{3.13}$$

With:

$$c = \sqrt{\frac{EI}{\rho wt}} \tag{3.14}$$

We can use separation of variables to solve the differential equation. Therefore, we are looking for solutions of the form:

$$y(x,t) = Y(x)T(t) \tag{3.15}$$

By inserting Equation 3.15 into Equation 3.13, and rearranging:

$$\frac{c^2}{Y(x)}\frac{\partial^4 Y(x)}{\partial x^4} = -\frac{1}{T(t)}\frac{\partial^2 T(t)}{\partial t^2} = \omega^2 \tag{3.16}$$

Both sides of the expression in Equation 3.16 must be equal to a common separation constant, ω^2. Then Equation 3.16 can be rewritten as two ordinary differential equations:

$$\frac{\partial^4 Y(x)}{\partial x^4} - \lambda^4 Y(x) = 0 \tag{3.17}$$

$$\frac{\partial^2 T(t)}{\partial t^2} + \omega^2 T(t) = 0 \tag{3.18}$$

With:

$$\lambda^4 = \frac{\omega^2}{c^2} = \frac{\rho wt\omega^2}{EI} = \frac{12\rho\omega^2}{Et^2} \tag{3.19}$$

The boundary conditions necessary to solve Equation 3.12 for a beam with one end clamped, one end free, and a concentrated load mass at the tip are:

$$y(0,t) = 0 \tag{3.20}$$

$$\frac{\partial y(0,t)}{\partial x} = 0 \tag{3.21}$$

$$\frac{\partial^2 y(l,t)}{\partial x^2} = 0 \tag{3.22}$$

$$EI\frac{\partial^3 y(l,t)}{\partial x^3} = M\frac{\partial^2 y(l,t)}{\partial t^2} \tag{3.23}$$

The first two conditions are geometrical constraints at $y = 0$, and the last two are the conditions for the unforced solution to the natural frequency at $y = l$. Equation 3.22 states that there is no bending moment at the free end of the cantilever. And Equation 3.23 shows that there is a shearing force on the beam at $y = l$ as a result of the end load mass, given by the mass times the acceleration. The boundary conditions must be transformed for use with the ordinary differential equations.

Therefore, upon examination of Equation 3.17, we can notice that the characteristic spatial frequencies are $\pm \lambda$ and $\pm i\lambda$. And the general solution for Equation 3.17 is given by:

$$Y(x) = Acosh(\lambda x) + Bsinh(\lambda x) + Ccosh(\lambda x) + Dsin(\lambda x) \tag{3.24}$$

Applying the boundary conditions derived from Equations 3.20 and 3.21, with $Y(0) = 0$ and $\frac{\partial Y(0)}{\partial x} = 0$ at the fixed end for $x = 0$ gives $A + C = 0$, and $B + D = 0$. This enables us to rewrite Equation 3.24 as:

$$Y(x) = A\big(cosh(\lambda x) - cos(\lambda x)\big) + B\big(sinh(\lambda x) - sin(\lambda x)\big) \tag{3.25}$$

Next we can apply the third boundary condition, Equation 3.22, with $\frac{\partial^2 Y(l)}{\partial x^2} = 0$.

$$\frac{dY(x)}{dx} = A\lambda\big(sinh(\lambda x) + sin(\lambda x)\big) + B\lambda\big(cosh(\lambda x) - cos(\lambda x)\big) \tag{3.26}$$

And:

$$\frac{dY^2(x)}{dx^2} = A\lambda^2\big(cosh(\lambda x) + cos(\lambda x)\big) + B\lambda^2\big(sinh(\lambda x) + sin(\lambda x)\big) \tag{3.27}$$

Therefore, applying the boundary condition gives at $x = l$:

$$B = \frac{cosh(\lambda l) + cos(\lambda l)}{sinh(\lambda l) + sin(\lambda l)} \tag{3.28}$$

We can then rewrite Equation 3.25 as:

$$\begin{aligned} Y(x) = A\big(cosh(\lambda x) - cos(\lambda x)\big) \\ + \frac{cosh(\lambda l) + cos(\lambda l)}{sinh(\lambda l) + sin(\lambda l)}\big(sinh(\lambda x) - sin(\lambda x)\big) \end{aligned} \tag{3.29}$$

And applying the last boundary, Equation 3.23, redefined as $EI\frac{\partial^3 Y(x)}{\partial x^3} = -M\omega^2 Y(x)$ for $x = l$, we can arrive at an expression for the allowable values of λ. Evaluating the third derivative of $Y(x)$ and substituting it into the boundary condition equation gives:

$$\begin{aligned} EIA\lambda^3\Big\{\big(sinh(\lambda l) - sin(\lambda l)\big) \\ + \frac{cosh(\lambda l) + cos(\lambda l)}{sinh(\lambda l) + sin(\lambda l)}\big(cosh(\lambda l) + sin(\lambda l)\big)\Big\} \\ = -M\omega^2 A\Big\{\big(cosh(\lambda l) - cos(\lambda l)\big) \\ + \frac{cosh(\lambda l) + cos(\lambda l)}{sinh(\lambda l) + sin(\lambda l)}\big(sinh(\lambda l) - sin(\lambda l)\big)\Big\} \end{aligned} \tag{3.30}$$

Further simplifying the expression:

$$\frac{M\omega^2}{EI\lambda^3} = \frac{1 + \cos(\lambda l)\cosh(\lambda l)}{\sin(\lambda l)\cosh(\lambda l) - \sinh(\lambda l)\cos(\lambda l)} \tag{3.31}$$

We can further examine the left side of Equation 3.31 by noting:

$$\frac{M\omega^2}{EI\lambda^3} = \left(\frac{\rho wt\omega^2}{EI}\right) l^4 \left(\frac{M}{\rho wtl}\right) \frac{1}{\lambda^3 l^3} \tag{3.32}$$

Comparing Equation 3.32 to Equation 3.19, and defining $\beta = \lambda l$, and $\alpha = \frac{M}{\rho wtl}$:

$$\frac{M\omega^2}{EI\lambda^3} = \frac{\beta^4}{\beta^3}\alpha = \beta\alpha \tag{3.33}$$

Therefore, we can now rewrite Equation 3.31 to obtain an expression for the discrete dimensionless eigenfrequencies, $\beta_n(\alpha)$. The value of β depends on the ratio of the load mass to the cantilever mass.

$$\alpha = \frac{1 + \cos(\beta)\cosh(\beta)}{\beta(\sin(\beta)\cosh(\beta) - \sinh(\beta)\cos(\beta))} \tag{3.34}$$

And from Equation 3.19, the angular resonant frequencies can be written as:

$$\omega = \lambda^2 t \sqrt{\frac{E}{12\rho}} \tag{3.35}$$

In terms of frequency, and substituting $\lambda = \frac{\beta}{l}$:

$$f_n = \frac{\beta_n^2(\alpha)}{2\pi} \frac{t}{l^2} \sqrt{\frac{E}{12\rho}} \tag{3.36}$$

The values for β can be solved numerically. The values for β_0 correspond to the fundamental mode, and β_1 to the second mode. Equation 3.36 and the values for β can be verified by

evaluating them for the case of no load mass, $M = 0$, meaning $\alpha = 0$. $\beta_n(0) = \{1.875, 4.694, \ldots\}$ in accordance with derivations of the simpler case without loading. Figure 3.15 shows values of β for the fundamental and second modes as a function of the ratio of load mass to cantilever mass, α.

Additionally, an effective value for β can be found when the mass of the pillar is ignored, and only the static bending stiffness and the mass of the load are used to calculate the resonant frequency. Starting with a variation of Equation 3.36, and setting it equal to the equation for resonance frequency in the case when the pillar mass is ignored:

$$\frac{\beta_{eff}^2}{l^2}\sqrt{\frac{EI}{\rho wt}} = \sqrt{\frac{k}{M}} = \sqrt{\frac{3EI}{l^3 M}} \tag{3.37}$$

Rewriting the expression:

$$\beta_{eff}^2\sqrt{\frac{EI}{\rho wtl^4}} = \sqrt{\frac{3EI}{l^3 M}} \tag{3.38}$$

Noting that the mass of the cantilever, $m = \rho wtl$:

$$\beta_{eff}^2\sqrt{\frac{EI}{l^4 m}} = \sqrt{\frac{3EI}{l^3 M}} \tag{3.39}$$

Therefore:

$$\beta_{eff} = \sqrt[4]{3/\alpha} \tag{3.40}$$

Figure 3.15 also contains another curve labeled quasi-static approximation, that represents β_{eff}. This curve shows the value of β required in Equation 3.36 that gives the same fundamental resonant frequency as the case where the cantilever is considered massless for the resonant frequency calculation. We can see that for $\alpha \geq 1$, the approximation given by Equation 3.40 matches the numerical soluton of Equation 3.34 quite closely. This intuitively makes sense, as

the mass of the load becomes substantial, and exceeds the cantilever mass, the β from Equation 3.24 should result in a resonant frequency similar to the equation for resonance with a massless cantilever.

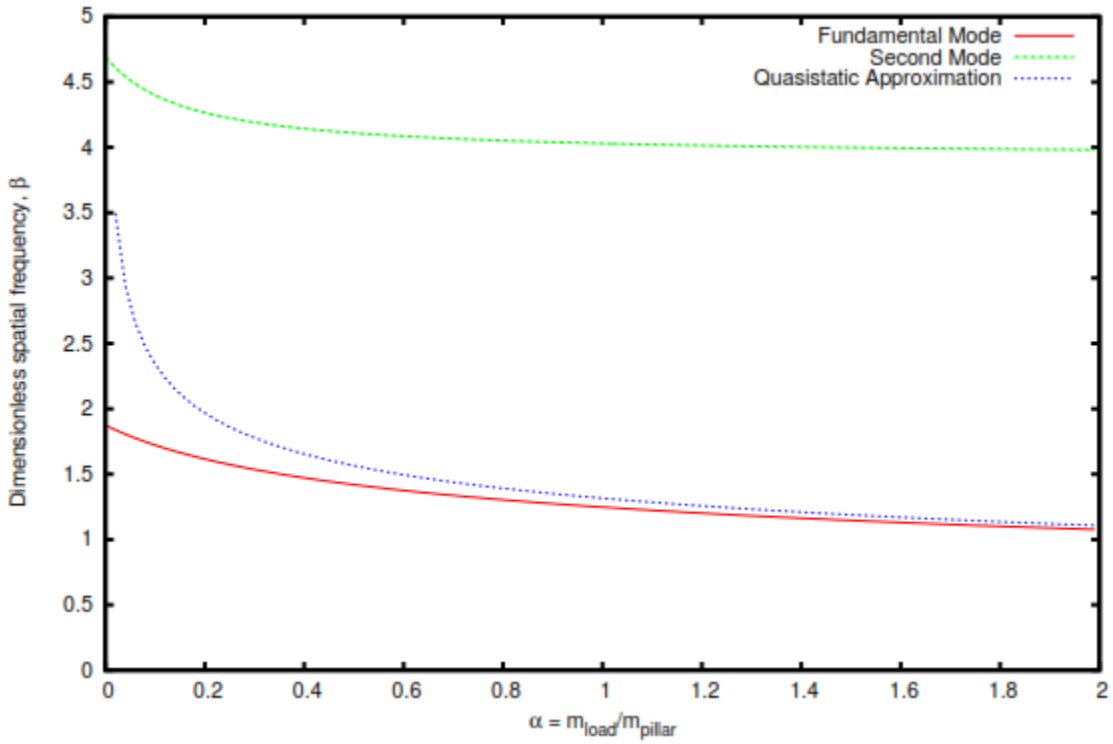


Figure 3.15: Dimensionless spatial eigenvalue, β, versus ratio of load mass to pillar mass, α. Eigenvalues are shown for fundamental mode and second mode for a loaded cantilever. The curve for the quasi-static approximation represents the effective β for the case where resonant frequency is calculated using the static bending stiffness and the mass of the load (ignoring the mass of the pillar).

Now that we have an exact expression for the resonant frequency of our pillar/Channel structure, we can take the absolute value of the resonant frequency measured optically, and extract the value for Young's modulus, *E*, using Equation 3.36. All other dimensions are known to the precision available through SEM evaluation. The volume of the metallic Channel, Si_3N_4 insulator with surrounding sidewall spacers, and the silicon within the sidewall, are evaluated by

rendering them in COMSOL with the dimensions collected from the SEM, as seen in Figure 2.14, and having the software calculate the respective volumes by accounting for rounded corners and sloped metal sidewalls, like those seen in Figure 2.33. The volume of the metallic Channel must be broken into its constituent parts, accounting for the different densities of the evaporated metal stack. For instance, the mass of the load (Channel) can be roughly calculated as, $M \approx \frac{1}{10}V_M\rho_{Al} + \frac{8}{10}V_M\rho_{Ti} + \frac{1}{10}V_M\rho_{Au} + V_{Si_3N_4}\rho_{Si_3N_4} + V_{Si}\rho_{Si}$, where V_M is the total volume of the metallic Channel, and the fractional volumes of the metals are estimated at $\frac{1}{10}, \frac{8}{10}, \frac{1}{10}$ for aluminum, titanium, and gold, respectively. The mass of the pillar can be calculated as, $m \approx W_{STEM}L_{STEM}H_{STEM}\rho_{Si}$. The ratio of the masses can be evaluated and the corresponding value of β can be found. We peformed the analysis for a number of nano-ribbon devices with different ribbon thicknesses.

Since silicon is an anisotropic crystalline material, the mechanical properties of a device depend on its orientation relative to the crystal lattice. Even bulk values for Young's modulus in single crystal silicon vary widely from 130 GPa in the <100> direction to 188 GPa in the <111> direction [62]. For a standard planar device with out-of-plane actuation, fabricated in (100) silicon, the value of Young's modulus used should be 130 GPa. Although our devices are fabricated in (100) silicon, the direction of motion for a vertical structure, fabricated either perpendicular or parrallel to the flat should be the <110> direction or an equivalent direction. Therefore, the bulk Young's modulus we should expect for our devices is 169 GPa [62].

Figure 3.16 shows the extracted values for Young's modulus as a function of nano-ribbon thickness. A clear trend in Young's Modulus is apparent, with Young's Modulus decreasing with lower thickness. At a thickness of ~ 200 nm, the Young's modulus reflects the bulk value

in single crystal silicon for the <110> direction. And at 120nm, the Young's modulus is almost half of its bulk value in silicon.

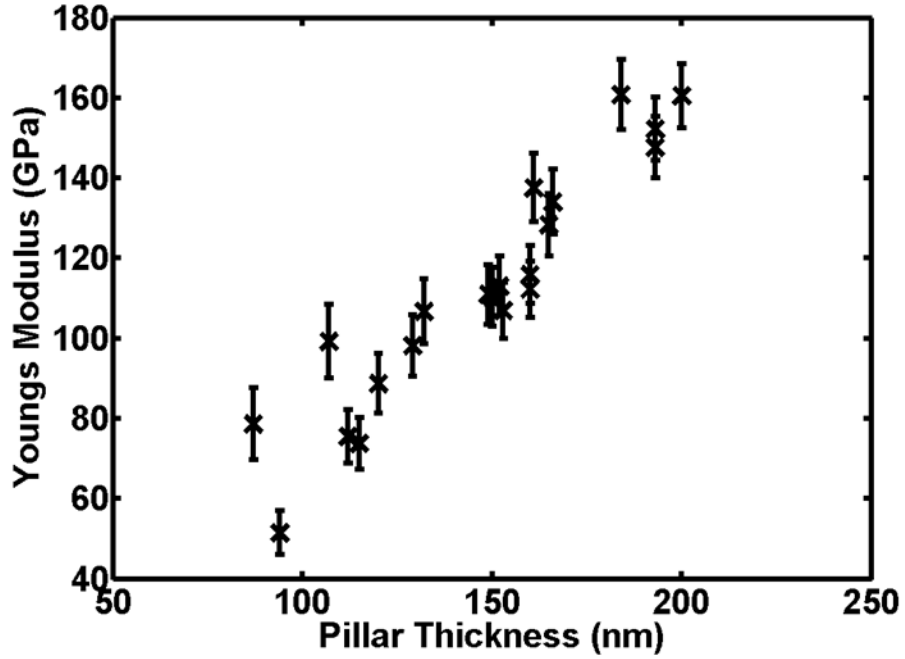
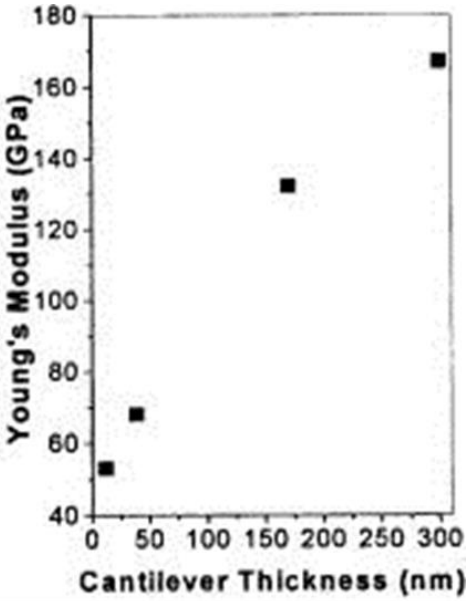


Figure 3.16: Extracted values for Young's modulus from resonant frequency data. Distinct decrease in Young's modulus noticeable for thin nano-ribbon devices.

Similar work using planar cantilevers made from SOI wafers was performed by X. Li, et al. SOI wafers enabled Li to have tighter control of the cantilever dimensions. A similar trend in Young's modulus is noticeable in the data shown in Figure 3.17. Then, by interpolating Li's data, and using it to fit our own resonant frequencies, we can have additional confirmation that a decreasing Young's modulus corresponds better with the experimental results. Figure 3.18 shows the experimental data for the measured resonant frequencies, with fits provided by Li's data for Young's modulus and the bulk value for silicon, ~ 170 GPa. The experimental data shows better accordance with a reduced value for Young's modulus over the full range of measured thicknesses.

Given the effect of size on Young's modulus, scaling of silicon based devices must take into account this nanoscale phenomena. Our analysis of device scaling in Section 2.7 included Young's modulus scaling. As noted earlier, although a decreased Young's modulus makes for lower voltage devices, it also decreases the restoring force for pull-out (turn-off) of the devices. However, this size effect in silicon can provide additional benefit to nano-scale device design and fabrication. Less aggressive scaling of nano-ribbon thickness will be necessary to achieve low voltage operation with decreasing Young's modulus. Therefore, nano-ribbon thickness can be kept slightly larger to offset the decreasing value for Young's modulus. This enables scaling to be less challenging, and also decreases the influence of other imperfections, such as silicon surface roughness and scalloping from deep etching.



X. Li et al., *APL*, vol. 83, no. 15, pp. 3081-3083, 2003.

Figure 3.17: Extracted values for Young's modulus as evaluated using cantilevers made from SOI wafers [78].

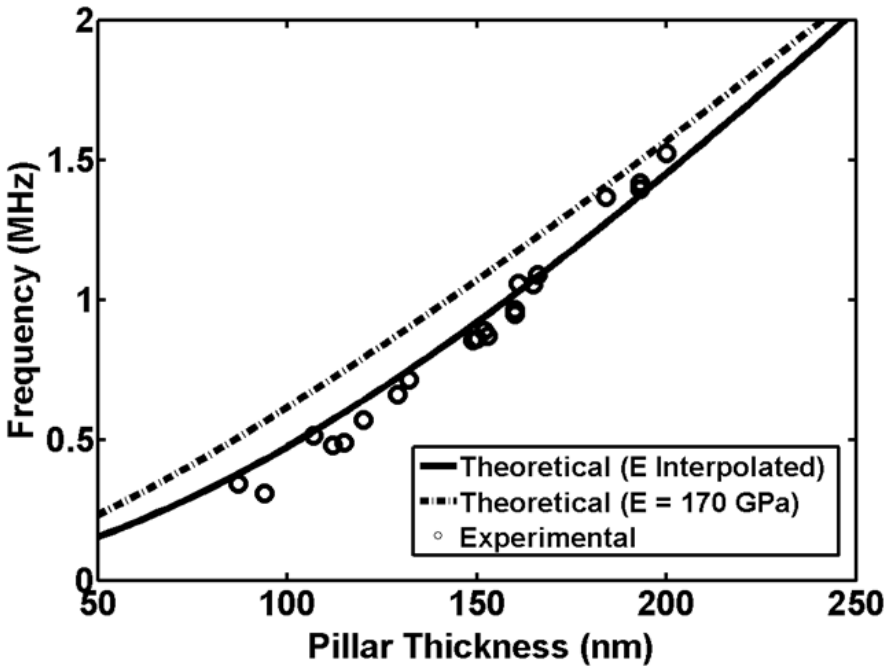


Figure 3.18: Using Li's data to fit our resonant frequencies, we confirm a decreased Young's modulus is present for these nano-ribbon devices.

3.4 ISSUES

Before attempting the optical measurement of the three terminal device, DC measurements were performed. Although a few devices showed switching behavior, the vast majority did not demonstrate any distinctive signs of switching. Upon observation in the SEM, a number of measured devices did appear to be permanently actuated, with the Channel adhered to either the Source or Drain. Switching behavior was not observed since the Channel only made contact with one electrode. After finding similar outcomes across numerous samples, it was determined that nano-ribbon device at the current design scale are unable to function when small offsets exist between the Source and Drain contacts, on the order of ~ 10's of nanometers, as seen in Figure 2.9. This conclusion leads to the torsion-based four terminal nano-relay.

CHAPTER 4

DESIGN/FABRICATION OF FOUR TERMINAL NEMS SWITCH

4.1 OVERVIEW

Having learned from the shortcomings of the three terminal vertical structure, this chapter will discuss the fabrication process, and device characteristics of a four terminal NEMS switch. The four terminal device will use torsion and bending to overcome the difficulties posed by practical device fabrication, thereby producing a more robust switch design, capable of handling larger process variations. Device designs will be explored based on the performance characteristics extracted from the three terminal structure. Results from DC measurement will show observable switching behavior from top down vertical structures. Device characteristics will also be analyzed using the optical measurement technique previously developed and discussed in Chapter 3. Additionally, simulations of the electrostatics and mechanics of the four terminal structure will be used to verify the experimental results for switching behavior. Analysis of the fabricated four terminal devices will lead to discussion of potential applications for this new class of structures.

4.2 FOUR TERMINAL FABRICATION PROCESS

The four terminal fabrication process follows a similar procedure to the three terminal design. A single optical lithography mask was used for the fabrication. Lithography was transferred from an i-line stepper (365 nm) to a DUV stepper (248 nm), with minimum feature

size of ~ 250 nm. A high quality quartz mask was used, thereby enabling better control of critical dimensions on the wafer, without the distortion introduced by over-exposure. Also, the same film stack was used, with essentially identical thicknesses. Standard LPCVD Si_3N_4 thickness was reduced to ~ 125 nm. And ~350 nm of undoped PECVD SiO_2 was deposited for the nitride sidewall process and the hard etch mask for the BOSCH process.

Two significant changes distinguish the four terminal mask design from the three terminal design, as seen in Figure 4.1. 1) A Gate terminal is introduced between the Source and Drain terminals, as discussed in Section 2.4. 2) The Channel shape is modified to have a non-uniform profile. The non-uniform profile comes into play during the size reduction step, as discussed in Section 2.7.2. The four terminal Channel is designed to change the shape of the silicon profile under the planar nitride layer during isotropic size reduction processes. The shape of Channel enables all the silicon to be cleared from under the narrow part of the Channel (except for the silicon protected by the nitride sidewall), while retaining silicon under the thicker part of the Channel. The result is that a ribbon-like structure transforms to nano-pillar structure offset to one side of the Channel, as seen in Figure 4.1. This is what enables torsion to be introduced into the structure.

In this structure, the sidewall process becomes even more crucial to device performance, as seen in Figure 2.17. In a torsion based device without the sidewall process, the capacitance between the Pillar and the Channel, C_{PC}, becomes increasingly small as the ribbon-like shape of silicon transforms to the pillar shape. Whereas the ribbon shape afforded some capacitive coupling to the substrate along the entire length of the Channel, the cross-sectional area of the pillar represents an extremely small portion of the total area of the Channel. Therefore, as the pillar size shrinks further, capacitive coupling reduces, and physical contact to the Channel from

the Pillar decreases when a sidewall process is not employed. The sidewall process naturally solves both of these difficulties. As with the three terminal device, the nitride sidewall protects the silicon covered by the sidewall, so that dimensions can be reduced without causing detriment to the electrostatics. Furthermore, while maintaining the capacitive coupling of the silicon substrate to the Channel, a much larger physical contact area is preserved between the planar silicon nitride layer and the silicon layer directly beneath it. This serves two important purposes, as illustrated in Figure 4.2. 1) A strong connection between the Pillar and the Channel can be maintained for small pillar thicknesses, thereby increasing reliability during pull-in and impact. 2) The thickness of the silicon underlying the planar nitride greatly contributes to the overall mechanical stiffness of the Channel. With a planar silicon nitride layer of ~ 125 nm alone, stresses in a ~ 300 – 400 nm evaporated metal film atop the nitride can cause deformation of the nitride and misalignment of the Channel to the Drain (with Pillar towards the Source side). However, a sidewall process creates a composite structure, with an upside down U-shaped nitride casing, and a silicon interior, thereby forming a stiff platform for thick metallization.

As with the three terminal device, lithography was also performed with a bilayer resist process. The bottom layer remained the liftoff resist, Shipley LOR 3A, and the top layer became Rohm and Haas UV 210 – 0.3. We used a very high spin speed for LOR 3A, ~ 5500 RPM, to keep the thickness down and prevent excessive over-development (undercutting) of small features. The main differences in the fabrication process occurred in the silicon etching steps: the shallow etch for the nitride sidewall, the deep etch for forming the nano-pillar, and the silicon isotropic size reduction process. Improved processes were developed for each of these steps, as will be discussed in this section.

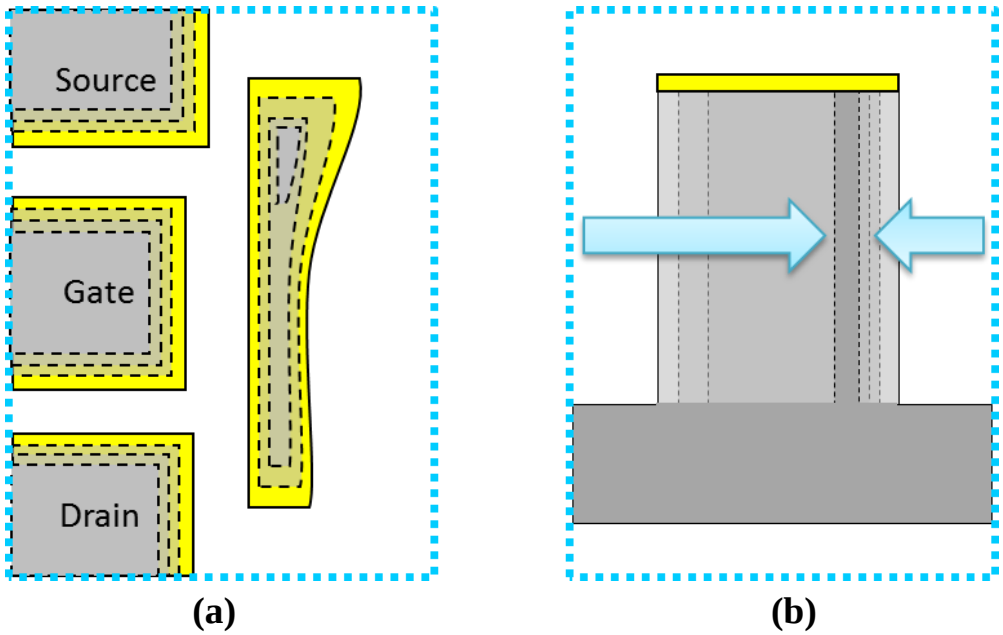


Figure 4.1: Fabrication and design changes of four terminal switch. (a) A Gate terminal is introduced between the Source and Drain electrodes. Top-view shows a non-uniform Channel profile. Dotted lines illustrate silicon profile change under planar nitride during size reduction. (b) Cross-section along length of Channel shows transformation from a ribbon-like shape to a pillar during size reduction step.

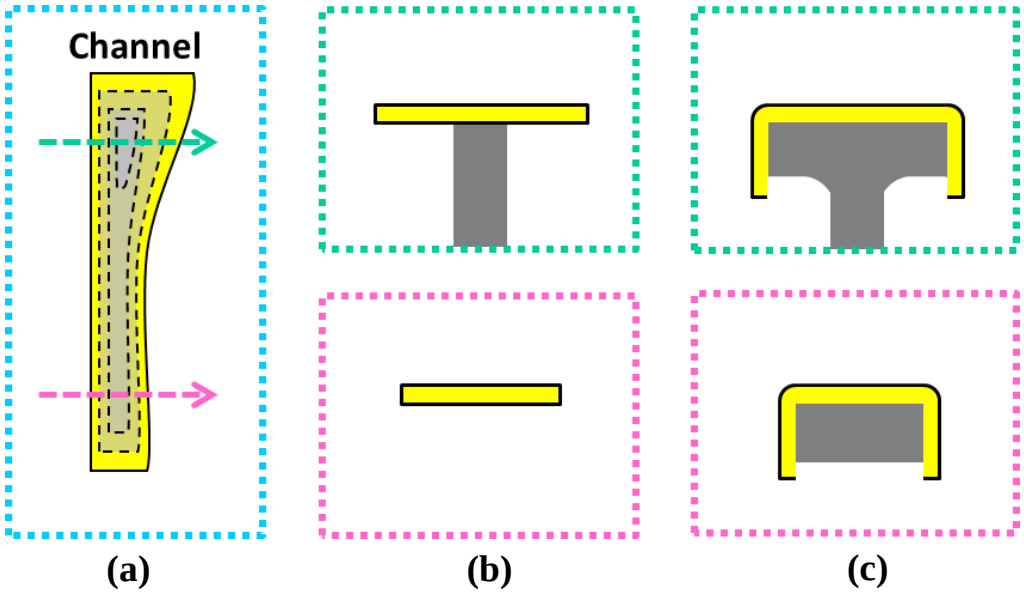
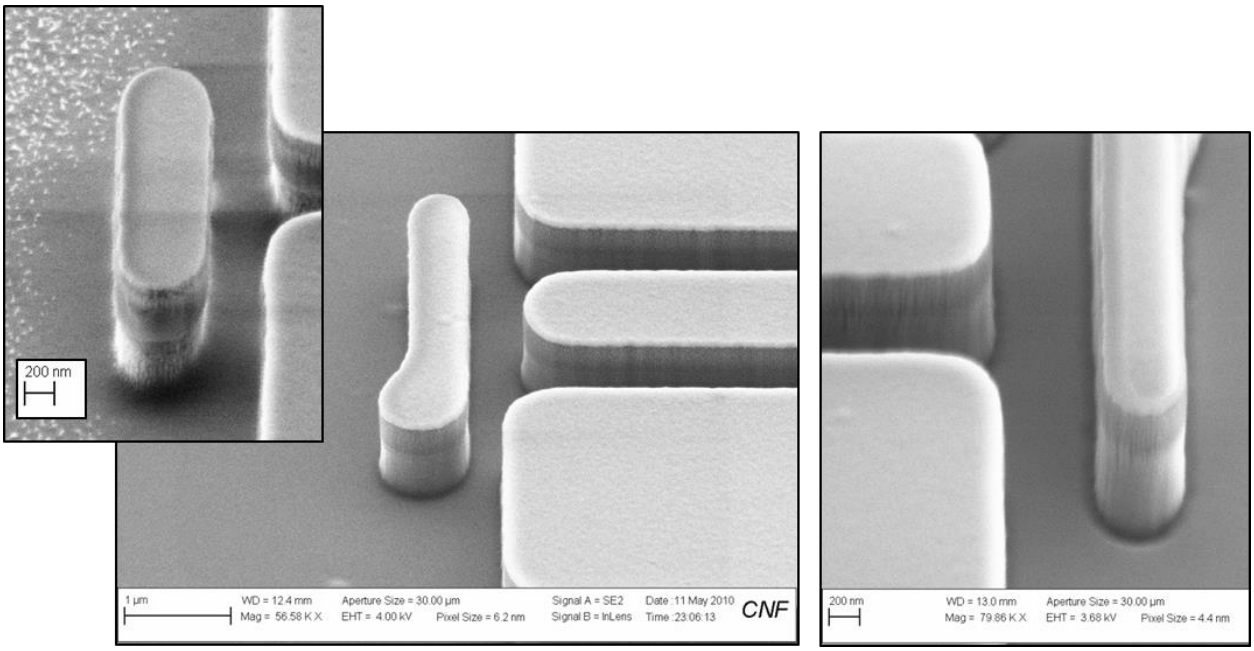


Figure 4.2: Schematic illustrating benefit of sidewall process for torsion-based device. (a) Top-view of Channel with two cut-lines for cross-sectional schematics. (b) Cross-section of Channel for structure without sidewall process. Top schematic shows Pillar coupling and physical contact to planar nitride. Bottom schematic shows region of Channel with no underlying silicon. (c) Cross-section of Channel for structure with sidewall process. Top schematic shows increased physical contact area of silicon to nitride. Bottom schematic shows increased thickness of Channel region throughout entire Channel.

Previously, a parallel plate reactor with CF_4 chemistry was used to transfer the pattern into the $SiO_2/Si_3N_4/Si$ stack (Figure 3.1, step 2). The four terminal device uses CF_4 chemistry with an inductively coupled plasma (ICP) etcher to achieve smoother sidewalls, and a more vertical etch. Figure 4.3 shows the results of using the ICP etch to perform the shallow etch. Figure 4.3(a) shows a 5 minute etch in CF_4 chemistry at a forward power of 15 W, for a total etch of ~ 850 nm. Figure 4.3(b) also shows 5 minutes of CF_4 etching, however, 25 W of forward power was used in an attempt to make a more vertical sidewall. Total etch depth was ~ 1050 nm for the higher power etch. From the inset in Figure 4.3(a), it can immediately be seen that the ICP etch provides smoother sidewalls, particularly in silicon. Vertical sidewalls with silicon in CF_4 chemistry is generally challenging, with the typical tendency of features to broaden as the etch proceeds. A slight footing is noticeable at the bottom of the silicon in Figure 4.3(a). The forward power was increased in an attempt to correct for this slight footing, as seen in Figure 4.3(b). Although the etch with 25 W forward power went ~ 200 nm deeper, the sidewall profile appears as vertical, if not more, over the entire height of the feature, as compared to the shallower etch with 15 W forward power. Additionally, the Cr etch mask seems to hold up even with higher forward power (higher DC bias). As noted previously, the verticality of the shallow etch is extremely crucial to proper metallization in devices with nitride sidewalls.

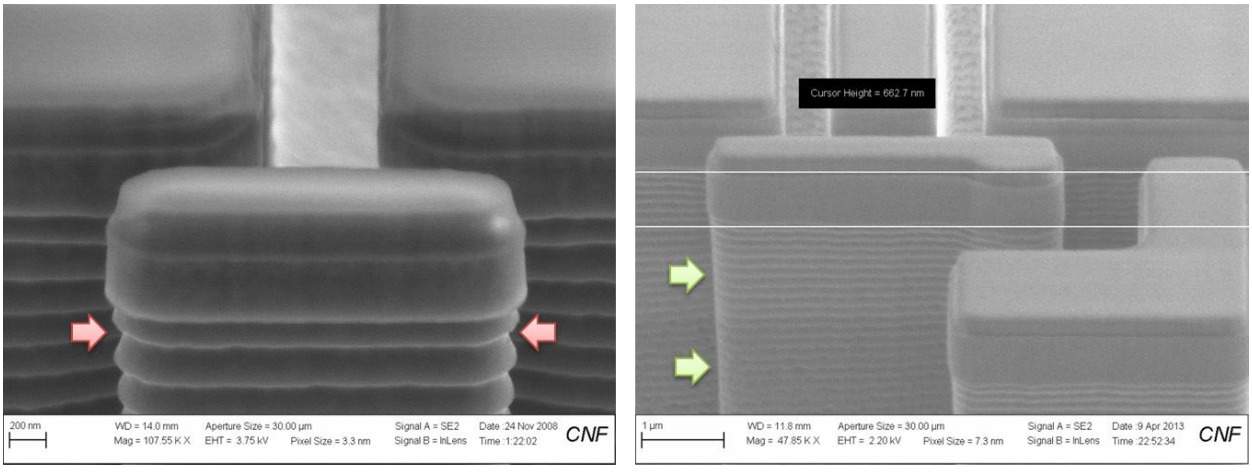
One of the difficulties mentioned in regard to the three terminal structures was scalloping from the BOSCH deep etch (Figure 3.1, step 5). Previously the Plasmatherm Unaxis 770 tool was used to perform the deep etch. A more recent deep etcher, the Plasmatherm Versaline tool, became available during the fabrication of the four terminal structure. Figure 4.4 shows the difference in etch profiles created by the two tools. The newer tool produces a distinctly smoother etch, by virtue of its shorter process cycles. Whereas the Unaxis etches ~ 9 μm in 27

cycles, the Versaline etches approximately the same depth in 44 cycles of the BOSCH process. Other deep silicon etches have been developed, mostly for applications in micro-optics, that result in high aspect ratio structures with ultra-smooth sidewalls. One such process is the cryogenic etching of silicon. Although it uses SF_6 for etching like the BOSCH process, the sidewall passivation mechanism is different. Whereas the BOSCH process uses a fluorocarbon polymer to coat the sidewall, the cryogenic process uses a blocking layer of oxide/fluoride (SiO_xF_y) on the sidewalls. The silicon etch product from the SF_6 etch, SiF_x, condenses on the sidewalls and combines with reactive oxygen to create the passivation layer [103]. Therefore, this process is not cyclical like the BOSCH the process, and smoother sidewalls are possible. Cryogenic temperatures inhibit attack on the passivation layer by fluorine radicals. Additionally, the fluorine radicals etch by chemical means and are sensitive to temperature, whereby selectivity to masking materials can also be improved [104]. The cryogenic process is a potentially better option for structures at the current size scale and smaller. However, with further scaling, other etches may become available that are currently being developed for Finfet technology and the like. Even wet etching of silicon using TMAH has resulted in high aspect ratio fins with heights of ~ 1.1 μm and sub-30 nm thicknesses by using crystallographic based etching [105]. Ultimately, etches with less scalloping will result in smoother pillars with more uniform thickness and smaller final dimensions. These advanced etching techniques will enable vertical top-down structures to be scaled to dimensions beyond planar NEMS structures and bottom-up structures being considered for nanoscale switching applications.



(a) **(b)**

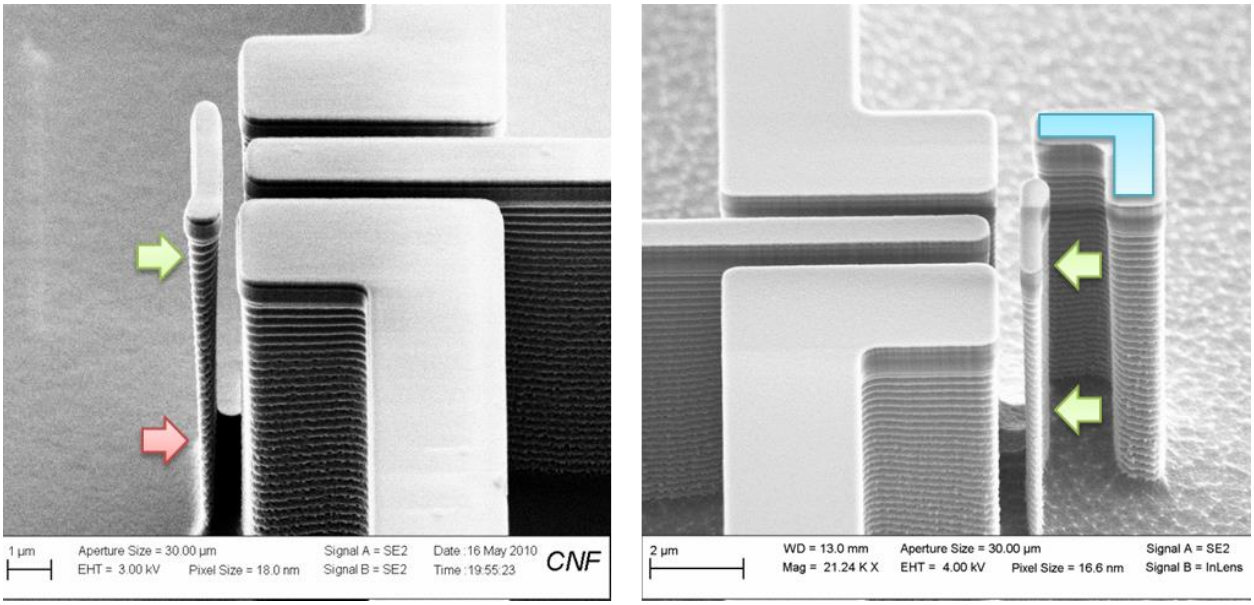
Figure 4.3: Shallow etch for nitride sidewall process using inductively coupled plasma (ICP) etcher with CF_4 chemistry. (a) Large image shows ICP etch with 15 W of forward power. Inset shows previous shallow etch in similar film stack with parallel plate reactor. ICP etch has smoother sidewall surface overall. (b) ICP etch with 25 W of forward power. Less footing can be seen at the bottom of the feature.



(a) **(b)**

Figure 4.4: SEM images demonstrating scalloping from BOSCH deep etch using different etchers. (a) Etch results for Plasmatherm Unaxis 770 tool. Older tool produces larger scallops. (b) Etch results for Plasmatherm Versaline tool. Etch uses shorter loops to substantially decrease scalloping.

One of the key features of the four terminal design, the non-uniform Channel profile, also posed a challenge to deep etching. The most aggressive designs, with the pillar region only ~ 150 nm larger than the narrow region of the Channel (~ 400 nm), were intended to produced thin pillars with minimal over-etching to clear the silicon under the narrow region. Given the tight tolerances, the deep etch must transfer the form of the Channel into the substrate, with consistent and uniform dimensions. However, in Figure 4.5(a), the pillar region is seen to taper and narrow as the etch proceeds. This etch profile prevents isotropic silicon size reduction. The bottom of the pillar pinches off during silicon removal, thereby making it difficult to remove the silicon under the remainder of the Channel for torsion-based operation. Deep reactive ion etching is known to have pattern dependent characteristics, particularly etch rate dependence [106]. Microloading is described as an interdependency between the etch rate and aspect ratio of features [107]. Here we see that a vertical structure exhibits similar issues. The side of the Channel with the Source, Gate, and Drain in close proximity displays a relatively vertical etch profile. However, the side without any nearby features shows tapering (undercut). The solution is seen in Figure 4.5(b). An L-shaped dummy structure is incorporated in the mask design. The structure was placed at a much further distance than Source/Drain spacing to the Channel to minimize the impact of the structure on the electrostatics of the device. The presence of this structure straightens out the sidewall profile in the pillar region of the Channel. A nearly vertical sidewall can be seen from the side view of the structure in Figure 4.5(b).



(a) **(b)**

Figure 4.5: SEM images demonstrating the effect of geometry on the nano-ribbon/pillar profile. (a) First attempt at torsion-based device. During BOSCH deep etch, wider region of channel becomes thinner with depth, quickly approaching thickness of thinner channel region. (b) L-shaped dummy structure introduced. Proximity effect on loading of etch causes thick region of Channel to have uniform dimensions with depth.

Whereas the three terminal device used oxidation and wet etching to reduce the critical dimensions of the structure, four terminal device fabrication employed the plasma etch size reduction technique discussed in Section 2.7.2.3. The main benefits, as summarized from the previous discussion are: avoidance of sidewall deformation during oxidation and high temperature processing, prevention of stiction by circumventing wet processing with high aspect ratio features, and process time savings. Numerous hours of oxidation and critical point drying can be replaced by a few minutes of dry etching. In actuality, oxidation was not entirely avoided. The BOSCH polymer posed as a large obstacle to size reduction with plasma processing. The teflon-like material was not easily removed using the wet or dry processing available. Therefore, a short oxidation was used to oxidize the silicon beneath the polymer. The sample was loaded at 650 ˚C, and ramped to 1000 ˚C over a 90 minutes interval, keeping the

ramp rate to less than 5 ˚C/min to enable gradual outgassing from the PECVD oxide mask. After 50 minutes of dry oxidation, ~ 50 nm of thermal oxide was grown. Subsequent removal of the oxide in buffered oxide etch was found to eliminate the remnants of the BOSCH polymer, leaving a clean surface. No critical point drying is required at this stage with wet processing since the structure is still relatively stiff, having not undergone substantial size reduction. Other low temperature techniques have been proposed for removing the BOSCH polymer. One such method requires using a high density radical flux, capable of achieving radical densities up to a 1000 times greater than conventional inductively coupled plasma sources [108]. Surface cleanliness was found to be extremely critical for the plasma etch size reduction technique with SF_6/O_2 chemistry. Figure 4.6 shows an image of a typical device after size reduction, prior to metallization. Initial results show tapering of the nanopillar towards the bottom of the feature. Optimization is required to produce nanopillars of uniform thickness. The pillar profile is tuned by the initial deep etch profile and the isotropic SF_6/O_2 etch. Both steps can be used to compensate for one another. Finally, metallization is performed using e-beam evaporation, as it was for the three terminal device. Figure 4.7 shows the four terminal device after metallization. Although these devices have a narrower Channel than the three terminal devices, the structure shows no deposition of metal on the silicon pillar itself. The size reduction not only serves to decrease the stiffness of the structure, but it also recesses the pillar within the Channel. Therefore, the pillar is not within line of sight of the e-beam source during evaporation. Additionally, the silicon nitride sidewall remained clear from deposition during the evaporation.

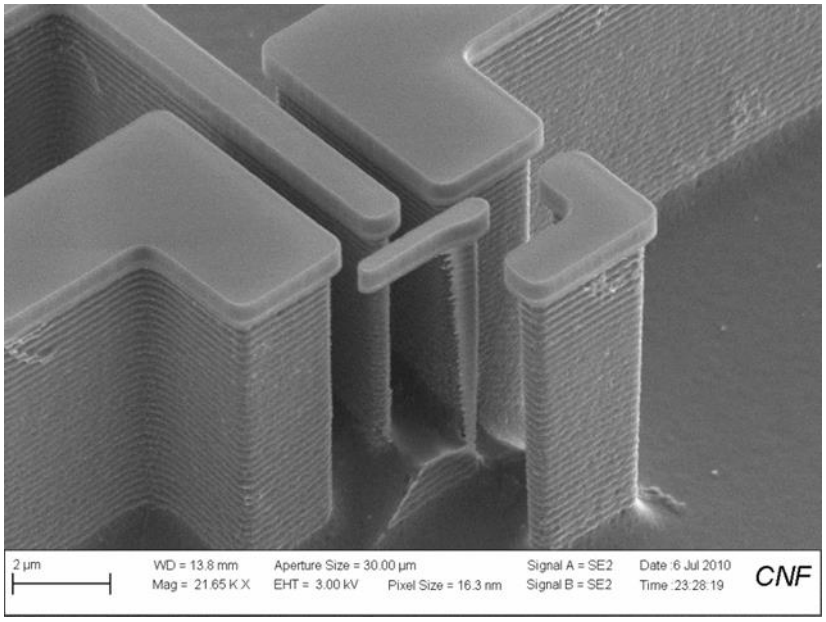


Figure 4.6: Typical result from SF_6/O_2 isotropic silicon size reduction process. All silicon clear from under narrow region of Channel. Thin silicon pillar remains, offset to one side of the Channel.

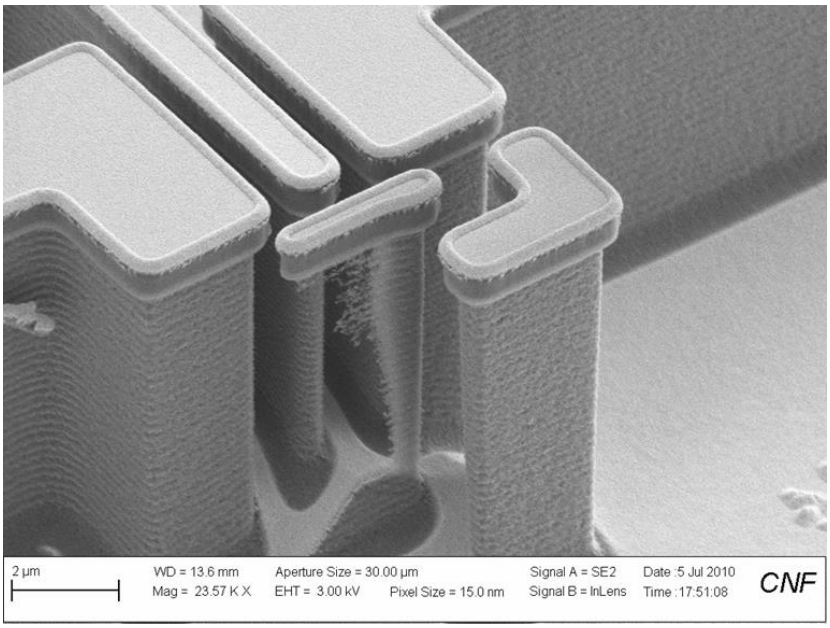


Figure 4.7: Four terminal structure after thick metallization. Thin strands of silicon can be seen protruding from the pillar, remnants of the isotropic silicon size reduction process. Silicon nitride sidewalls appear clear from metal deposition.

4.3 DEVICE CHARACTERISTICS

Having obtained a nano-pillar type structure with Channel affixed to the top, the device was placed in the optical measurement setup discussed in Chapter 3.3 to analyze its AC behavior and to explore the bending and torsional modes of the structure. The first resonance was found at ~ 330 kHz, and corresponds to the bending mode of operation. Figure 4.8 shows the frequency spectrum of the device exhibiting the fundamental mode of operation. Additionally, the dimensions of the silicon pillar under measurement are outlined. From a similar device in Figure 4.7, it can be seen that the pillar width and length are both non-uniform and vary along the height of the pillar. The pillar is more wide and thick at the top compared to the bottom. Upon exploring higher frequencies, a second resonance was observed at ~ 2.6 MHz. Figure 4.8 shows the torsional mode of operation for the same device displayed in Figure 4.7. Comsol simulation was used to verify the mode shapes and resonant frequencies of the measured device. Figure 4.10(a) illustrates the structure used for modal analysis. The design attempts to account for many of the non-idealities seen in the fabricated structure of Figure 4.7. The variations in pillar width and thickness make simulation a better option for analysis. These dimensional variations were included for accurate determination of the bending and torsional stiffness of the pillar. The model also accounts for the relevant mass contributions. The metallization was included with its slope sidewalls, and also the mass of the nitride sidewalls and the silicon they encapsulate. Figure 4.10(b) and (c) show the simulated fundamental and second mode. The simulated fundamental mode occurs at a frequency of ~ 370 kHz and displays a bending mode of operation. The simulated second mode occurs at a frequency of ~ 3 MHz and displays a torsional mode of operation. The first two modes show good agreement with the measured

resonances. The lower frequency mode for this device displays bending operation given that L_{STEM} is smaller than W_{STEM}.

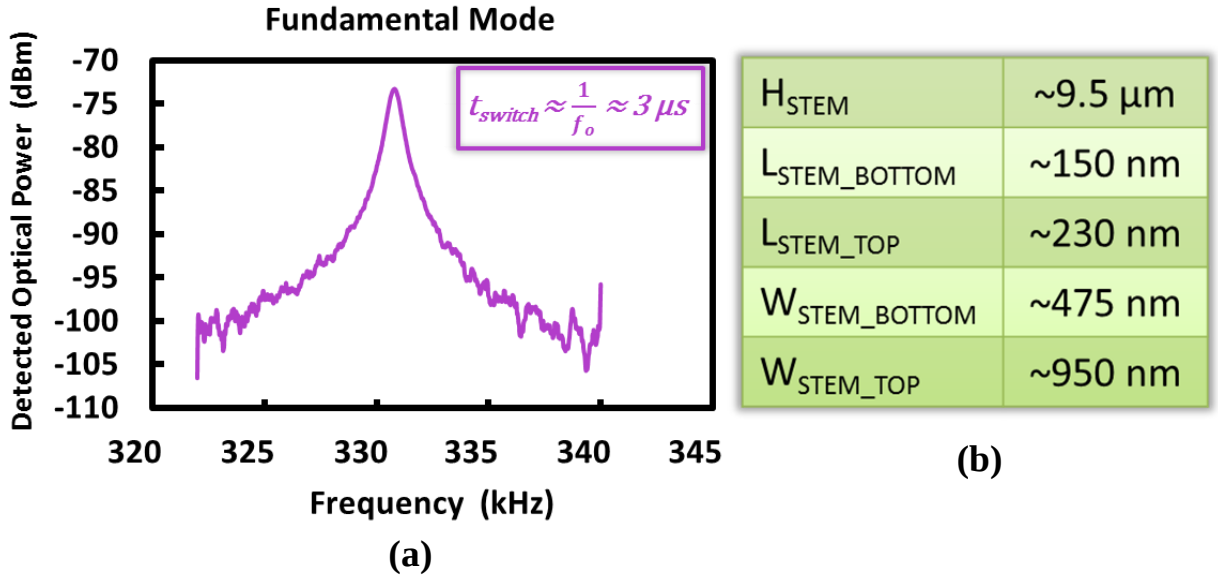


Figure 4.8: Optical measurement of four terminal device in vacuum setup using knife-edge technique. (a) Detected optical power reflected from the torsion-based device. Resonance appears at ~ 330 kHz. (b) Pillar dimensions of four terminal device under optical measurement. Pillar has non-uniform dimensions along its height.

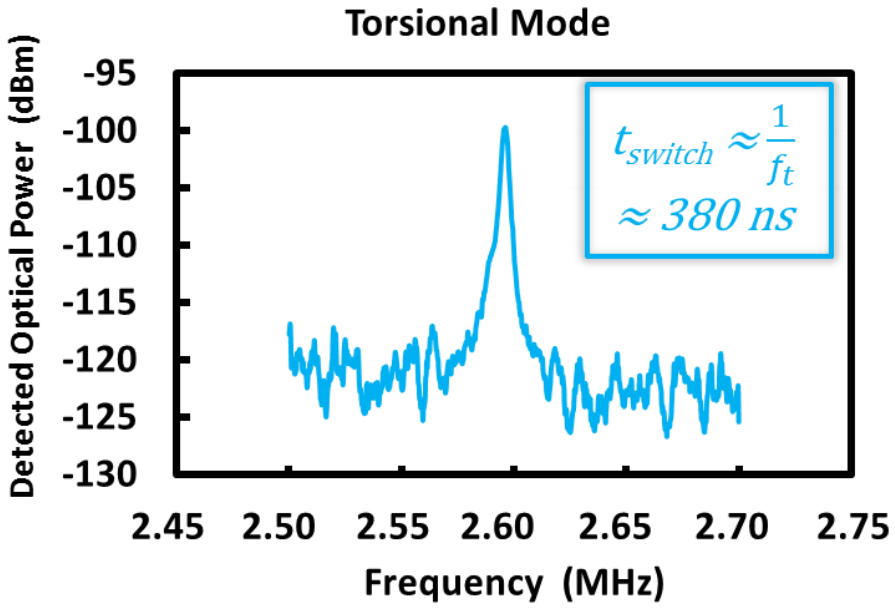


Figure 4.9: Optical measurement of four terminal device in vacuum. Detected optical power reflected from the torsion-based device. Second detected resonance appears at ~ 2.6 MHz. This resonance corresponds to the torsional mode of excitation.

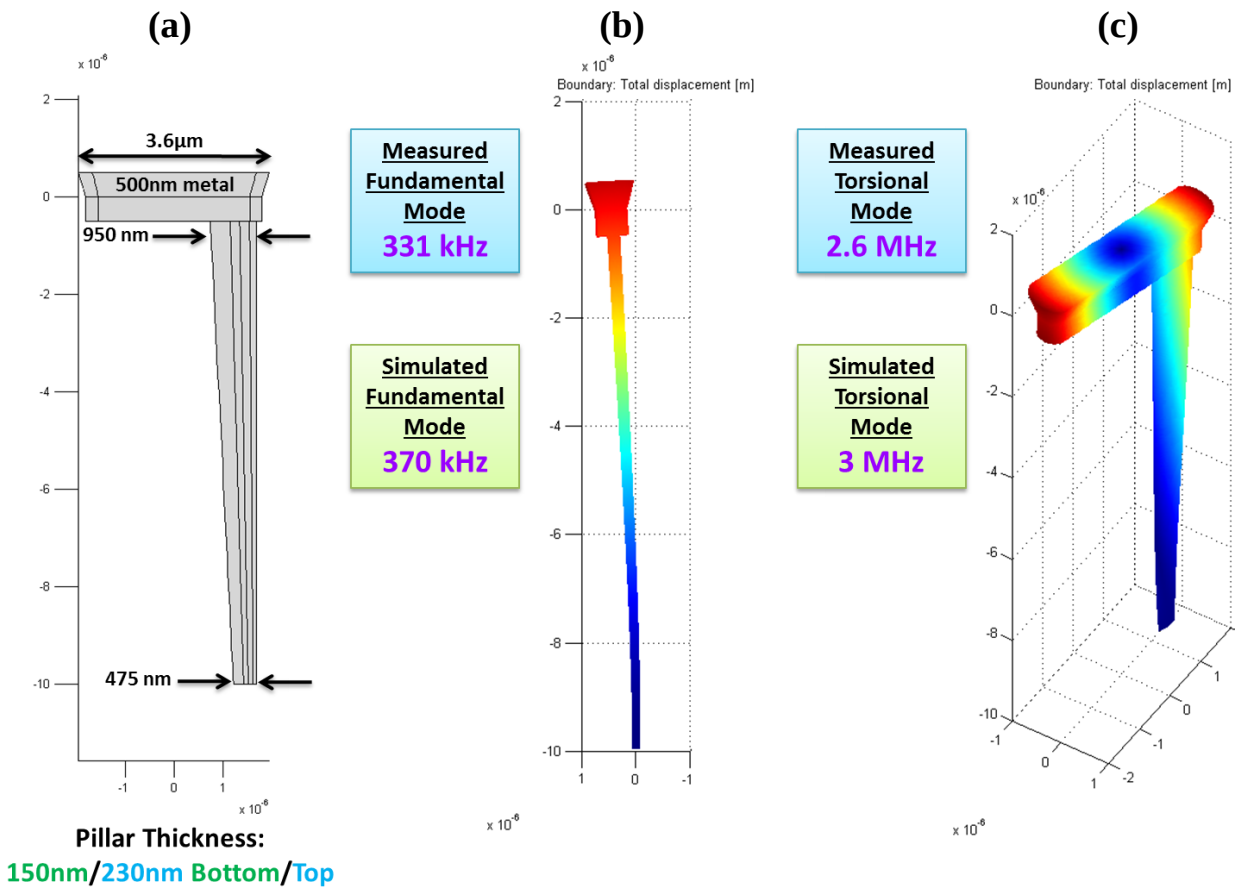


Figure 4.10: COMSOL simulation using modal analysis. (a) Model used for eigenfrequency analysis. Schematic includes non-uniform thickness and width, metallization with sloped sidewalls, and silicon nitride sidewall with enclosed silicon. (b) Side-view of simulated fundamental mode. Mode characterized by bending. Simulated mode frequency is ~ 370 kHz. (c) Second mode shows torsional profile with frequency at ~ 3 MHz.

Having designed the four terminal device to account for typical values of line edge roughness and surface roughness, DC characterization was performed to analyze the switching behavior of the vertical structure. Measurements were executed with the Source and Pillar/Substrate grounded, and Drain biased at a low voltage, V_D = 0.1 V. A small Source – Drain voltage was used in attempt to prevent large current flow during operation, which leads to Joule heating, micro-welding and permanent adhesion. Figure 4.11 shows a four terminal device abruptly switching at ~ 10 V. The dimensions of the pillar are L_{STEM_BOTTOM} ≈ 130 nm, and L_{STEM_TOP} ≈ 180 nm. The device had a rather large air gap of ~ 230 nm. The switch only

demonstrated one switching cycle. Figure 4.12 shows an SEM image of the device after actuation. Irreversible adhesion of the Channel to the Source and Drain can be seen. The device remains in a permanently actuated state, with Source and Drain electrically connected.

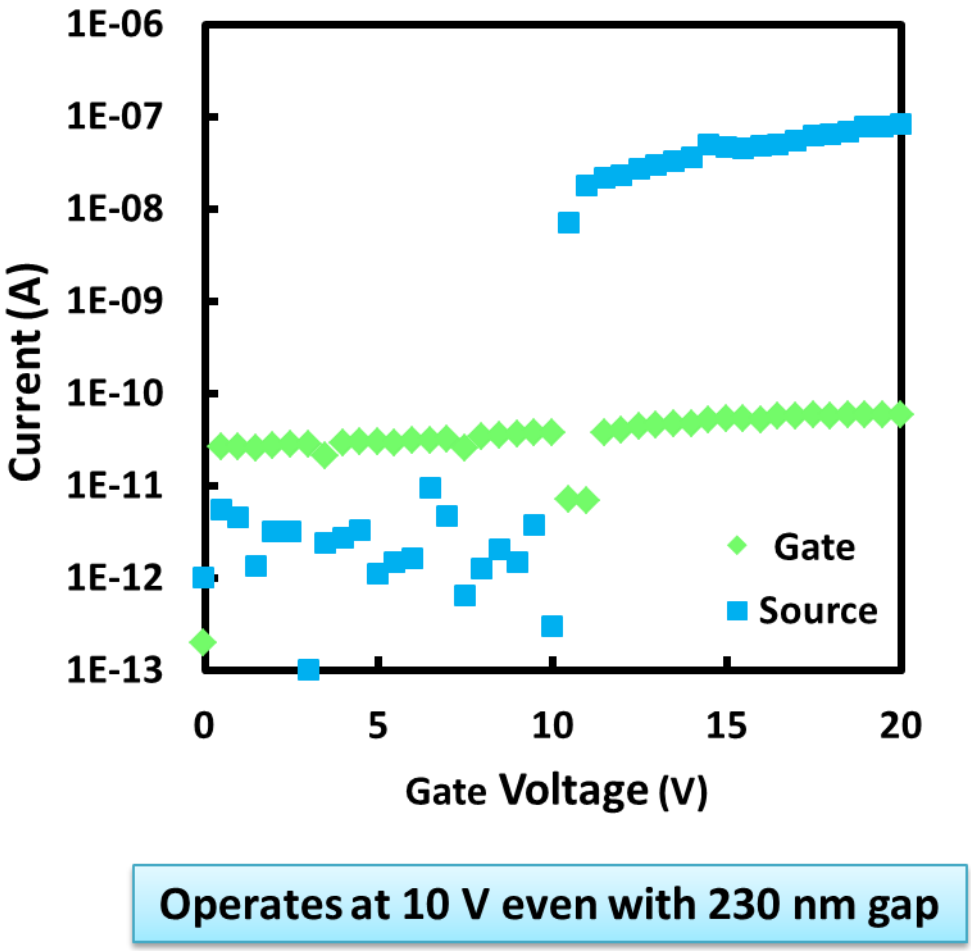


Figure 4.11: DC characterization of a four terminal device. Device has a gap ≈ 230 nm, L_{STEM_BOTTOM} ≈ 130 nm, and L_{STEM_TOP} ≈ 180 nm. The drain voltage, V_D = 0.1 V, and V_S = V_P = 0 V.

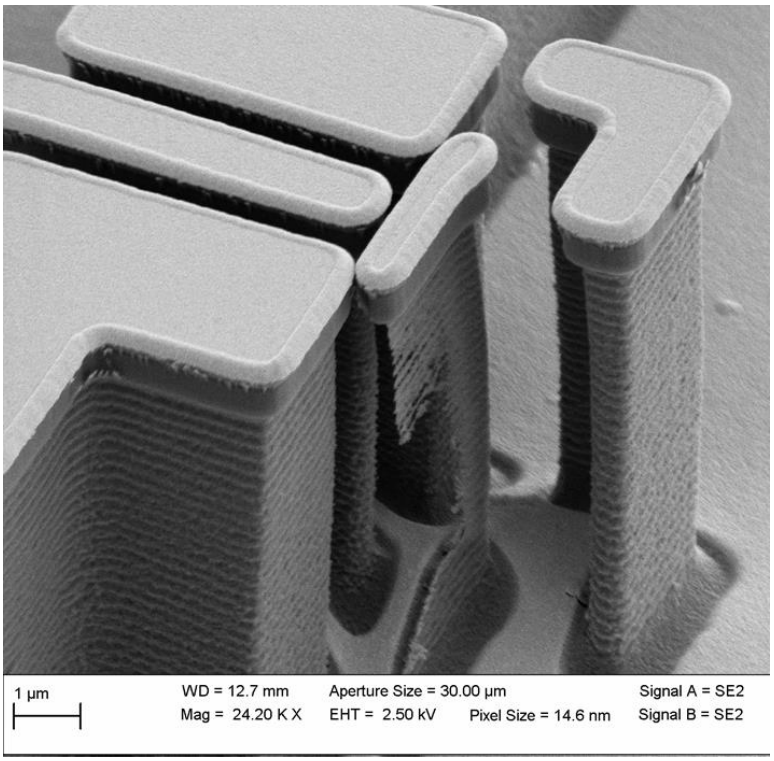


Figure 4.12: SEM image of device used for DC characterization. Device in the image pulled-in at 10 V. Switching behavior was not observable after one sweep. Device can be seen to be permanently attached to the Source and Drain.

Additional devices were measured, many of which exhibited higher pull-in voltages and single cycle operation. The initial DC voltage sweep of another device of interest is shown in Figure 4.13. The first sweep shows turn-on at ~ 19.5 V, with biasing conditions identical to the previous device. However, Figure 5.14 shows repeated sweeps for the same device. The structure continues to exhibit switching behavior. However, the operation voltage is shifted to a lower voltage, ~ 15.5 V. Observation in the SEM of the device shows the Channel pinned to the Drain, with a small gap, ~ few 10's of nanometers, still between the Channel and Source, as seen in Figure 4.15. From this image it is possible to conclude that the device is operating purely in a torsional mode. However, the higher initial operation voltage in Figure 4.13 suggests that the device operation was first limited by bending operation. After a larger pull-in voltage due to bending was achieved, lower voltage operation in a torsional mode was enabled by a much

smaller gap and single capacitor operation with the drain bias pinning the Channel potential through physical contact. At this point the device resembles a three terminal structure, as discussed in Section 2.4.2. With switching characteristics demonstrating bending and torsional-based operation, a new method of operation and programming can be suggested. If the bending mode of operation is designed to function at a lower voltage than the torsional mode, then the device can theoretically undergo initial pull-in without turning on the switch. Therefore, the devices can be designed to have a stiff torsional mode and a compliant bending mode so that fabrication can be performed with large initial gaps, useful for lithography and deep etching, and then be made to undergo a pre-programming state. Thereby, all switches can be made to operate with smaller gaps and lower voltages in the torsional mode. All that is required is a predefined Source – Drain offset to ensure that devices will not make contact with both the Source and Drain upon bending pull-in. Additionally, the bending stiffness must be low enough to enable Van der Waals forces or micro-welding to cause adhesion at the initial point of interaction.

Another important feature noticeable in the DC characteristics is the high value for resistance in the on-state. With on-currents in the range of ~ 1 – 100 nA's for V_{DS} = 0.1 V, switch resistance is in the range of ~ 1 – 100 MΩ. These high resistances are problematic for practical switching applications, and most NEMS switching devices have shown resistances on the order of MΩ to GΩ [25]. A number of carbon nanotube based devices have shown lower resistances, ~ kΩ's [25]. However, a NEMS switch based on a gold cantilever with gold electrodes, used for analyzing nano-scale contacts, demonstrated on-state resistances from 83 Ω to 640 Ω, and current handling ability > 1 μA [37]. Calculations of Au-Au contacts using a model based on contact at a single asperity resulted in contact resistance values between 15 and 209 Ω's [37]. The analysis accounts for the radius of the contact region and the deformation of

the contact upon impact. Contact resistance is determined to be governed by ballistic transport for nano-scale contact switches, and physical contact can result in elastic or plastic deformation depending on the impact velocity. Although the measured Au-Au contacts had higher experimental resistance, most likely due to environmental factors and contamination, the low values for resistance indicate the potential for efficient and useful NEMS switches. The electrodes and contacts of the fabricated vertical four terminal switches are also capped with ~ 40 – 60 nm of Au. However, the resistance is still unusually high. The majority of deposited metal is titanium, with surface passivation at room temperature consisting of primarily TiO_2 [109]. Values of resistivity for TiO_2 can range from 0.1 – 10 Ω•cm for sputter deposited Ti in water vapor with rutile form [110]. TiO_2 is even considered for gate oxide replacement for its low leakage high-permittivity properties [111]. By contrast, sputtered Au has a resistivity of ~ 3.6 μΩ•cm [112]. Therefore, if Au is making contact to TiO_2, a much higher resistance would be expected. Figure 5.16 illustrates a potential explanation for a high resistance physical contact. Using geometrical arguments, bending of a slender cantilever can result in tip displacement perpendicular to the direction of motion, thereby aligning a thin Au top layer to a TiO_2 sidewall passivation layer.

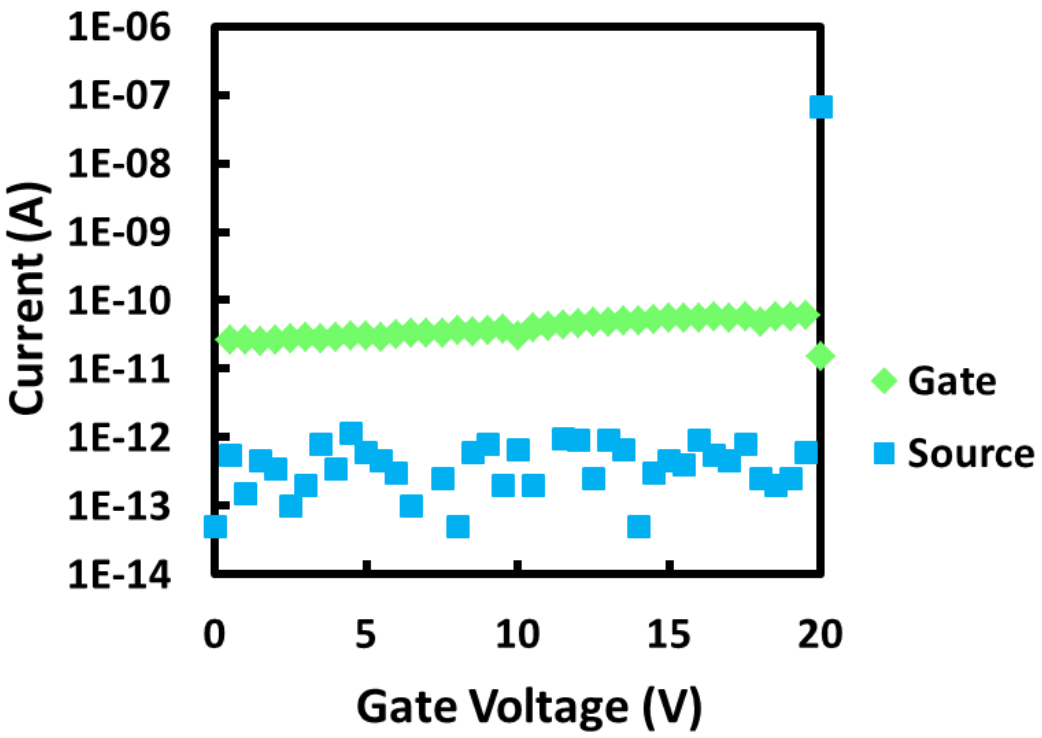


Figure 4.13: DC characterization of another four terminal device. Device demonstrates initial pull-in at 19.5 V. The drain voltage, V_D = 0.1 V, and V_S = V_P = 0 V.

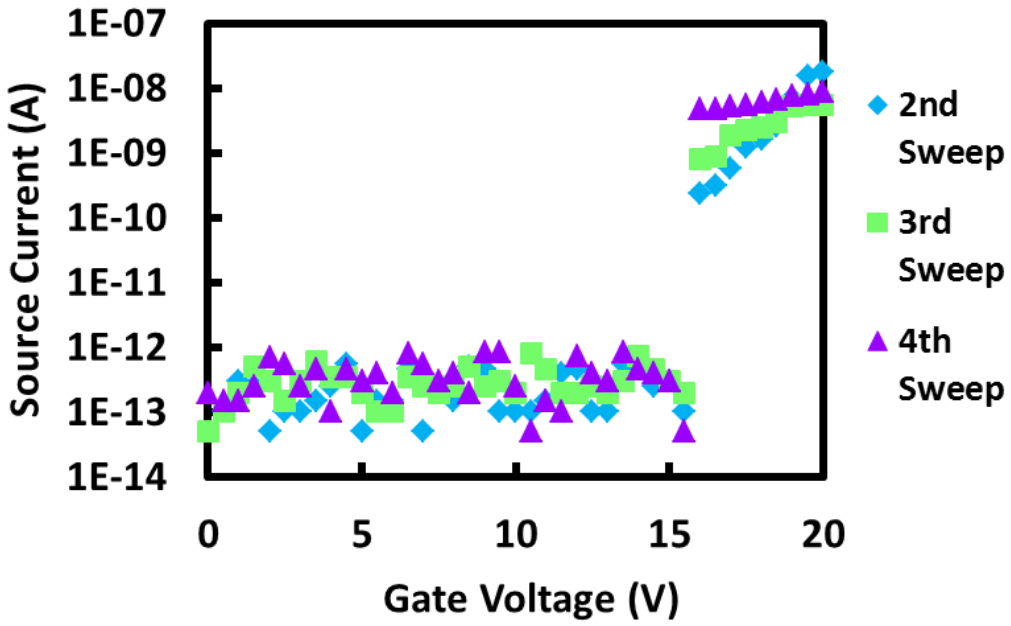


Figure 4.14: DC characterization of device in Figure 5.13 with repeated sweeps. Bias conditions remain V_D = 0.1 V, and V_S = V_P = 0 V. Resistance of device seen to decrease with repeated actuation.

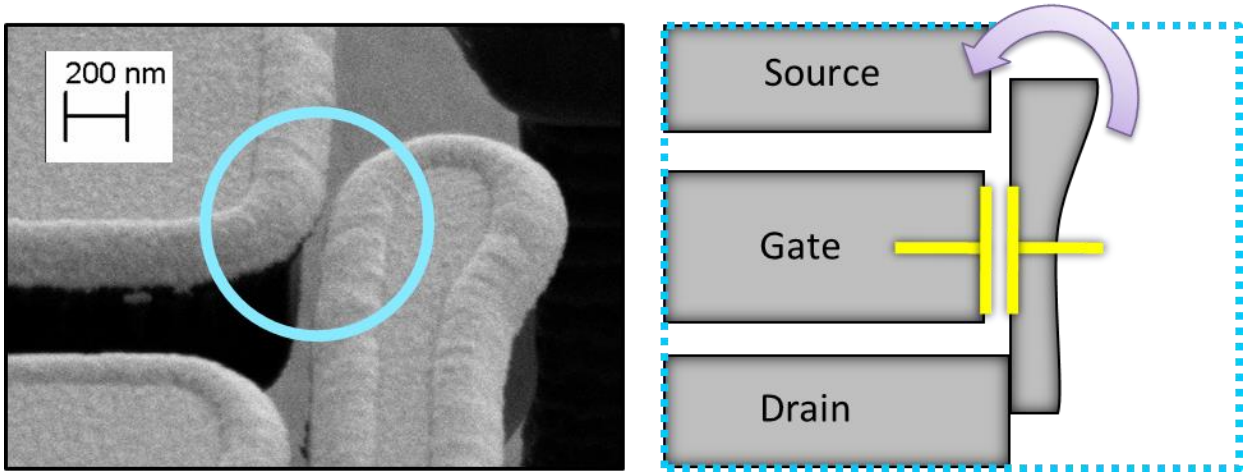


Figure 4.15: Verification of device mode of operation. (a) SEM image shows small gap between Source electrode and Channel, with other end of Channel pinned by the Drain (not shown). (b) Schematic of current operation of device. Switch operates in purely torsional mode with single capacitor configuration.

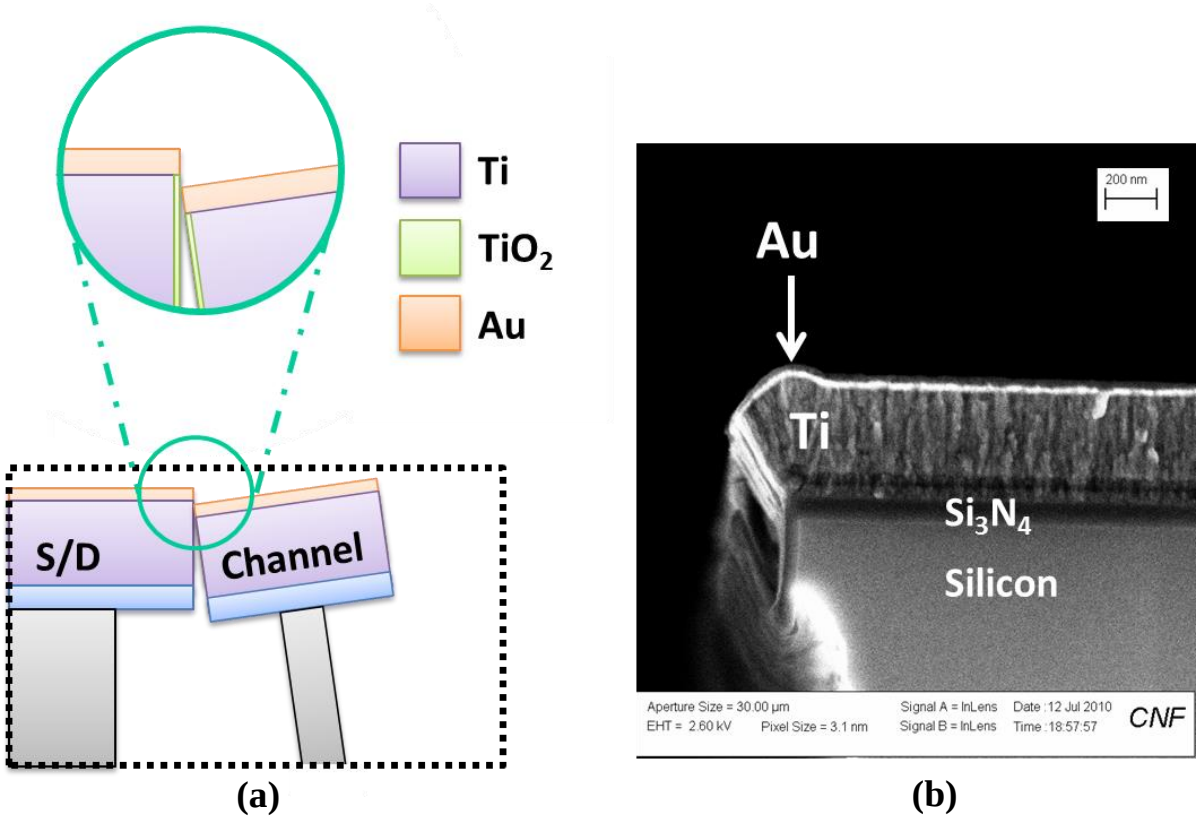


Figure 4.16: Potential explanation for high on-state resistance in four terminal devices. (a) Schematic of device after pull-in. For devices with thin Au cap and large gaps, geometry indicates potential for Au-Ti contact. (b) SEM image of thin Au layer atop thick evaporated Ti layer.

CHAPTER 5

3D INTEGRATION OF NEMS & ICs

5.1 OVERVIEW

If nanomechanical switches are to complement and enhance CMOS devices, a practical approach must be found for integrating these diverse technologies. Chapter 1 discussed a number of potential applications that could benefit from the low power operation of NEMS switches. Requirements on number of switching cycles, on-state resistance, and switching speed determine and limit the prospective applications that are currently available for NEMS. However, nano-relays can benefit applications such as FPGA routing switches, look up table implementations, power gating approaches, and device/circuit error correction at small scales. Nevertheless, to harness the advantage of nano-relays a method must be developed for interfacing NEMS with CMOS. The extreme complexity of CMOS design and fabrication suggests that NEMS switches should be fabricated on their own dedicated wafer. Research in 3D integration and chip stacking is paving the way for the merging of distinct technologies. A variety of chip/wafer bonding techniques have been developed for 3D integration. However, these methods do not address issues unique to nanomechanical devices. Mainly, how can bonding be performed for devices with nanoscale moving parts? Also, how will the topography of NEMS devices be handled by current bonding techniques? This chapter will review some of the work related to bonding and 3D integration. Additionally, a more robust four-terminal fabrication procedure will be developed for achieving large arrays of working switches. Moreover, a novel bonding technique will be presented for use with top-down vertical switches. This method will be of great value to planar NEMS as well.

5.2 BONDING IN 3D ICS

Numerous and diverse bonding processes exist. Although there are too many to discuss in depth, a brief discussion of bonding methods and selection criteria is possible. Three stacking schemes exist for 3D integration: chip-to-chip, chip-to-wafer, and wafer-to-wafer. Wafer-to-wafer provides the highest throughput and simplest process flow. However, it is most suitable for processes that have a high yield of individual good dies before bonding [113]. Another aspect, already mentioned in Chapter 1, is via-first and via-last processing. Via-first describes an approach to forming vias whereby the vias are built on each individual wafer before bonding. And via-last involves the building of vias after the wafers are already bonded. Via-first has traditionally been more efficient for through silicon vias (TSV) [114]. And finally, a bonding technology must also be chosen. Some of the possibilities include: anodic bonding, direct bonding (molecular bond/fusion), plasma activated direct bonding, glass frit, thermocompression, solder, eutectic, and adhesive bonding [115].

Selecting the appropriate bond will depend on the thermal budget, surface properties of the surfaces to be bonded (flatness and roughness), and alignment accuracy [115]. Other factors such as complexity and throughput can be significant for production considerations. Additionally, many of these processes are not CMOS compatible. Anodic bonding uses an applied electric field to assist diffusion of ions (typically Na+) across the bond interface. CMOS contamination by sodium ions can be of concern, and high voltages can cause damage to electrical structures [116]. Direct bonding relies on hyrophillic surfaces generated by we chemistry to result in van der Waals bonding. Thermal annealing is used to transition the weak van der Waals bonds to covalent bonds. A high temperature post-anneal of more than 800 ˚C is necessary to increase the bond strength of a silicon fusion bond, with bond strength approaching

that of bulk silicon for an anneal at 1000 ˚C [117]. Such temperatures cannot be considered for post-CMOS processing. Plasma activated direct bonding is a variation of direct bonding, where surfaces are pre-treated with oxygen plasma to increase surface reactivity and decrease the post anneal temperature. Glass frit bonds require the softening and flow of a glass intermediate layer at the bonding interface. Therefore, glass frit bond can take place at a somewhat moderate temperature. Thermocompression bonding uses heat and pressure to cause atomic diffusion between the bonding surfaces. Solder bonding is a particularly low temperature example of thermocompression bonding. Eutectic bonding (also a subset of thermocompression bonding) is achieved by using two materials that form a eutectic system (a mixture of elements that have a single chemical composition that results in a lower melting temperature than the individual elements). Eutectic bonds can achieve high bond strength at relatively low temperatures. Adhesive wafer bonding uses intermediate layers, consisting generally of polymeric materials, to connect or glue substrates.

Amongst all the bonding technologies, only thermocompression, solder, and eutectic bonding result in electrically conductive channels. These methods are the most widely used for 3D IC stacking. Metal-to-metal bonding techniques also help with heat dissipation throughout the stack. The most common choices for metal are Cu – Cu, Cu – Sn – Cu, Au – Au, Ti – Si, and In [118]. With proper choice of materials, bond and anneal temperatures can be kept below 400 ˚C. Further options exist within metal-to-metal bonding. Connections between interfaces can be achieved by micro-bumps or direct metal-to-metal bonding, amongst others. The concept of a micro-bump is derived from traditional and widespread use of large solder bumps (~ 100 μm diameter). For 3D chip stacking, solder bumps were reduced to a diameter of ~ 10 μm, as seen

in Figure 5.1 [119]. However, use of thick metal layers and achievable metal aspect ratios still limits the density of the micro-bump bonding approach.

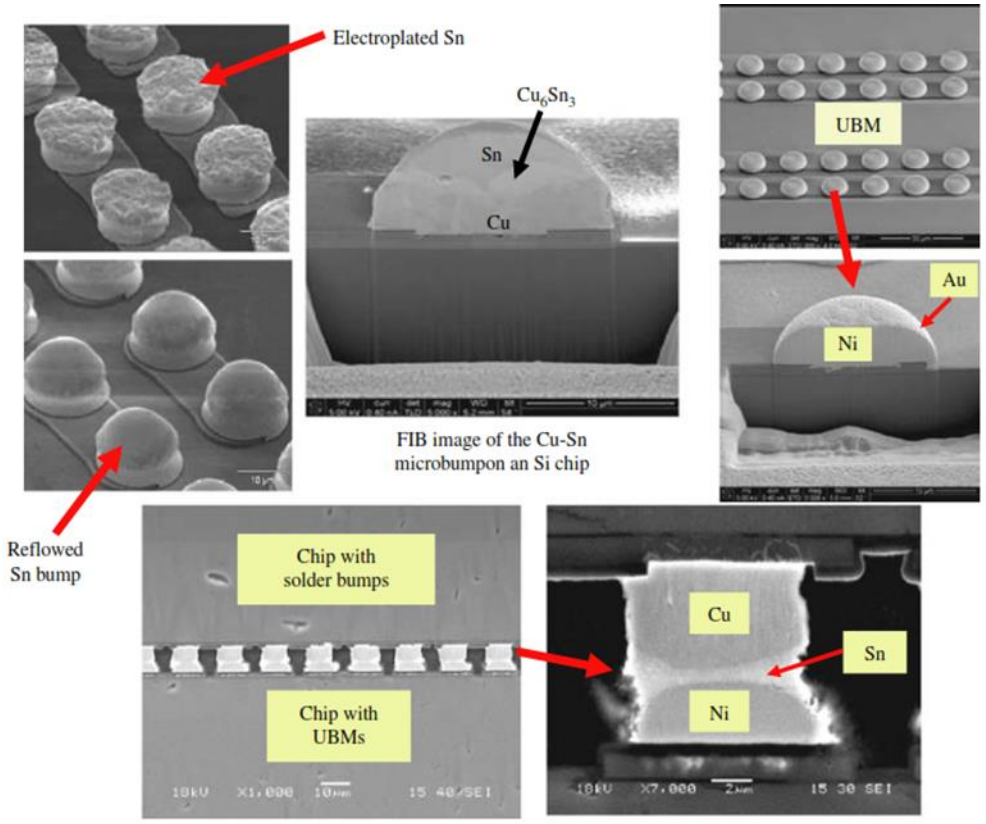
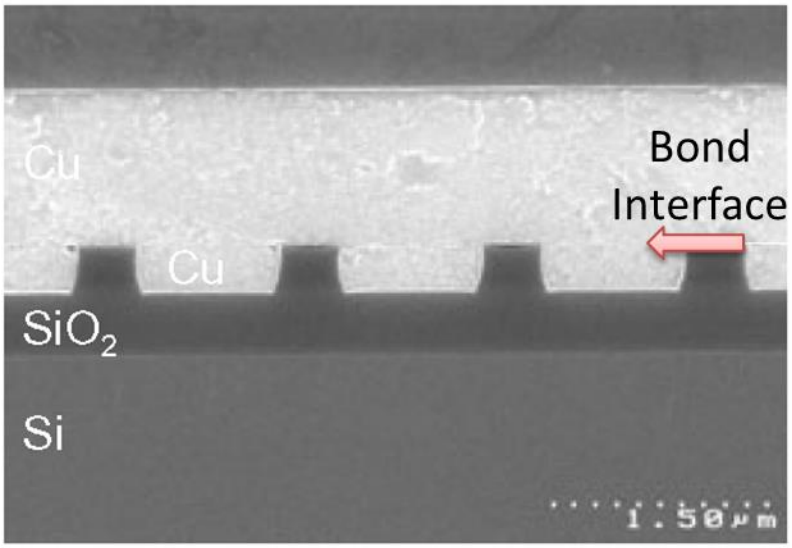


Figure 5.1: SEM images of a variety of micro-bumps before and after wafer/chip bonding.

Metal-to-metal bonding enables a higher density of interconnects/contacts than micro-bump bonding. One of the options being investigated is copper-to-copper bonding. Copper processing has already been developed for use with microprocessor interconnects. Copper bonding extends the usage of these mature processes to form thin and extremely planar copper surfaces (in terms of flatness and roughness) to enable void-free low resistance 3D interconnects at temperatures below 400 ˚C. Figure 5.2 shows a wafer with patterned features filled with

copper and bonded to a unpatterned wafer with copper. As deposited copper had a roughness of 15 nm RMS. After chemical mechanical polishing (CMP) roughness was reduced to 0.4 nm RMS. Hydrophobic copper surfaces were placed in contact at room temperature and atmospheric pressure. Post- bond annealing was performed at 300 ˚C [120]. The bond interface has essentially vanished for the small copper-to-copper bonded structures in Figure 5.2. In order to apply metal-to-metal bonding processes to nanomechanical devices, high standards for surface roughness and flatness will need to be achieved. This requirement could present a significant challenge for released mechanical structures with extensive topography.



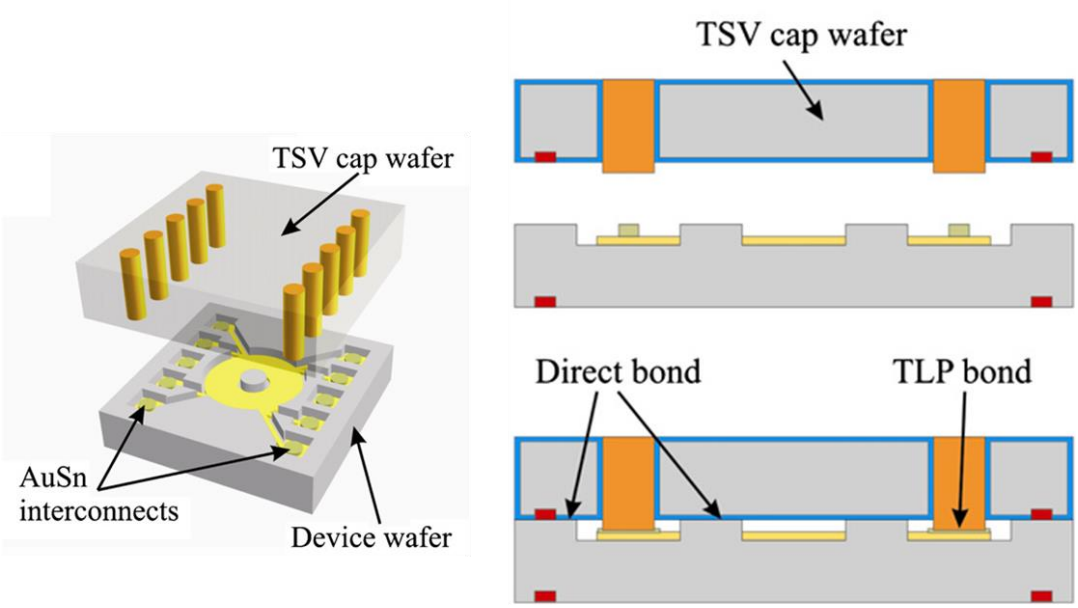
P. Gueguen et al., MINATEC, STMicroelectronics, 2008.

Figure 5.2: SEM image of a patterned wafer bonded to unpatterned wafer with copper. Annealing was performed at 300 ˚C. Small features were successfully bonded without voids.

5.3 OVERVIEW OF BONDING IN MEMS

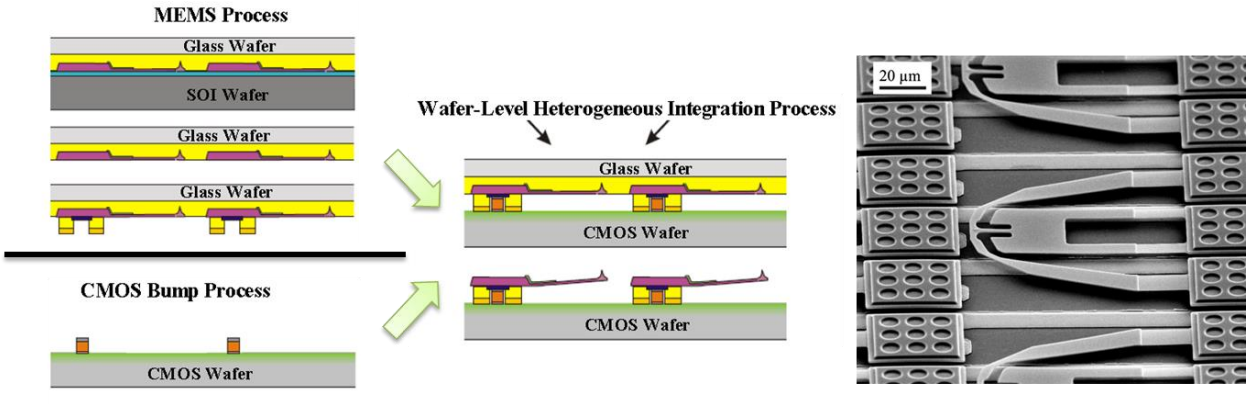
Wafer/chip bonding has been used in MEMS for microstructure formation and assembly [121], interconnects [122], and packaging/micro-encapsulation. Microstructure assembly can be achieved by bonding structural or electrical layers to a pre-existing structure. Individual components can be combined to form a completed MEMS structure, similar to the building of modular homes. Interconnects and packaging go hand in hand for MEMS devices. Many MEMS devices have strict requirements for environmental factors such as humidity and pressure. Therefore, hermetic packaging has been a major focus for MEMS devices. Nonetheless, electrical connections must be maintained with the MEMS device after encapsulation. A variety of interconnect approaches have been developed. One such approach relies on through silicon vias when employing a silicon encapsulation layer [123]. Figure 5.3 shows a method that uses a hybrid bonding scheme; whereby electrical interconnects are formed using transient liquid phase bonding (AuSn), while strong direct bonding enables cavity formation and careful alignment. Using plasma-activated direct bonding, both processes were carried while maintaining the temperature below 250 ˚C. A particularly well-known example of MEMS wafer bonding, demonstrated by IBM, can be seen in Figure 5.4. Instead of stacking multiple chips with devices, only the devices themselves were transferred. The bonding process simultaneously formed the anchors for the individual cantilevers and the electrical interconnects with the “CMOS” (dummy CMOS) below the cantilevers [124]. This method, along with similar approaches [125], uses interlocking structures on the two wafers to guide the alignment process. As bonding processes and alignment methods further improve, heterogeneous integration of NEMS and CMOS will be the method of choice. Unlike MEMS-last or MEMS-CMOS co-

fabrication (Section 1.4.2), 3D integration enables unparalleled freedoms in terms of substrate selection, fabrication processes, and thermal budget.



S. Kuhne and C. Hierold, ETH Zurich, 2011.

Figure 5.3: Use of silicon encapsulation with through silicon vias to form electrical interconnects while simultaneously creating strong direct bonds for cavity formation.



M. Despont et al., IBM, 2004.

Figure 5.4: Use of wafer-scale bonding for micromechanical device transfer and interconnection.

5.4 A ROBUST FABRICATION PROCESS

Before endeavoring to perform wafer/chip scale bonding of NEMS devices, a robust fabrication process is necessary, capable of producing large arrays of working devices. Without this precondition, it will be difficult to ascertain the effectiveness of the bonding technique and the effect that the bonding process has, if any, on the NEMS devices. Previous designs, discussed in Chapters 2 – 4, had varying degrees of success from batch to batch. One of the primary difficulties throughout the development of the vertical top-down switch was with the metallization process. Metal deposition on the silicon nitride sidewall invariably resulted in non-working devices. Although some methods had improved sidewall profiles, as mentioned in Section 2.7.2, device fabrication remained somewhat inconsistent. Therefore, a high yielding fabrication process is necessary to facilitate device and interconnect characterization irrespective of the bond process yield. Two different methods were pursued to achieve more consistent fabrication results. Both methods were aimed at suppressing line-of-sight (directional evaporation) deposition on exposed silicon nitride sidewalls. One method entirely removed the sidewall, and replaced it and the underlying silicon by a silicon dioxide layer. The other method retained the sidewall process; however, the sidewall angle was significantly changed. The desired outcomes of the two approaches are shown in Figure 5.5. The design without the silicon nitride sidewall requires simpler etching processes; however, it loses the mechanical and electrical benefits of the sidewall. The benefits, as mentioned in Section 4.2, include increased structural support for the Channel and larger capacitive coupling of the pillar to the Channel. Therefore, the device with angled sidewalls is a superior structure on many accounts. The following sections will describe in more depth these improved fabrication processes.

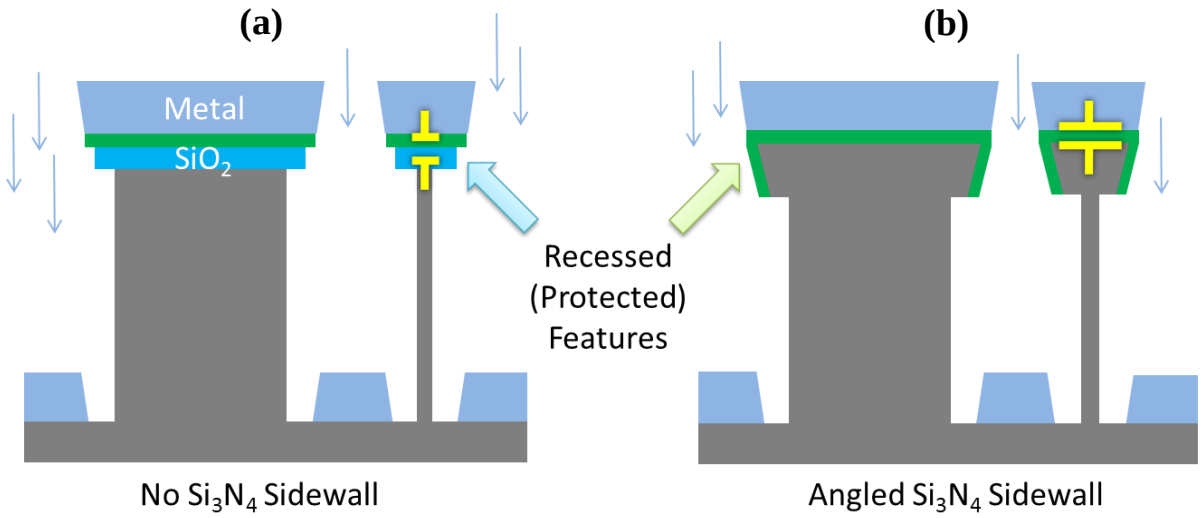


Figure 5.5: Two methods for fabricating vertical structures suitable for thick metallization by evaporation. (a) Schematic shows recessed silicon dioxide structural layer beneath planar silicon nitride layer. (b) Schematic shows structure with angled (recessed) silicon nitride sidewall.

5.4.1 Four-Terminal Device without Sidewall

The structure without the silicon nitride sidewall resolves the metallization issue by introducing a silicon dioxide layer beneath the planar silicon nitride layer, as seen in Figure 5.5(a). However, if the oxide layer was flush with the nitride layer, metal would deposit on it just as it does to the structure with the nitride sidewall. Since the evaporant is not a true point source with respect to the mounted samples, some evaporation is inevitable even on the sides of vertical structures. Therefore, the simplest solution is to recess the thick structural layer (SiO_2) so that it is truly protected from the evaporant during metallization. When using a Si_3N_4 sidewall process, the Cr etch mask (Figure 5.6, Step 2) must be removed before depositing Si_3N_4 in a CMOS clean furnace. However, in this process, the Cr etch mask is used to etch the Si_3N_4, SiO_2, and bulk Si. After deep silicon etching, a thin SiO_2 layer is grown to remove the BOSCH polymer and recondition the silicon surface (Figure 5.6, Step 4). This SiO_2 must be sufficiently thin (~ 40 – 50 nm) such that removal of the SiO_2 will be possible without excessively undercutting the planar SiO_2. Using BOE 30:1, a timed etch was performed to simultaneously

remove the SiO_2 of Step 4, and form the necessary undercut in the planar SiO_2 (Figure 5.6, Step 5). Next, an additional thin Cr evaporation (~ 10 nm) was performed to protect the planar Si_3N_4 layer during the SF_6/O_2 etch in Step 7. SiO_2 has excellent selectivity to Si in SF_6/O_2. And finally metallization was performed without difficulty, as seen in Figure 5.7.

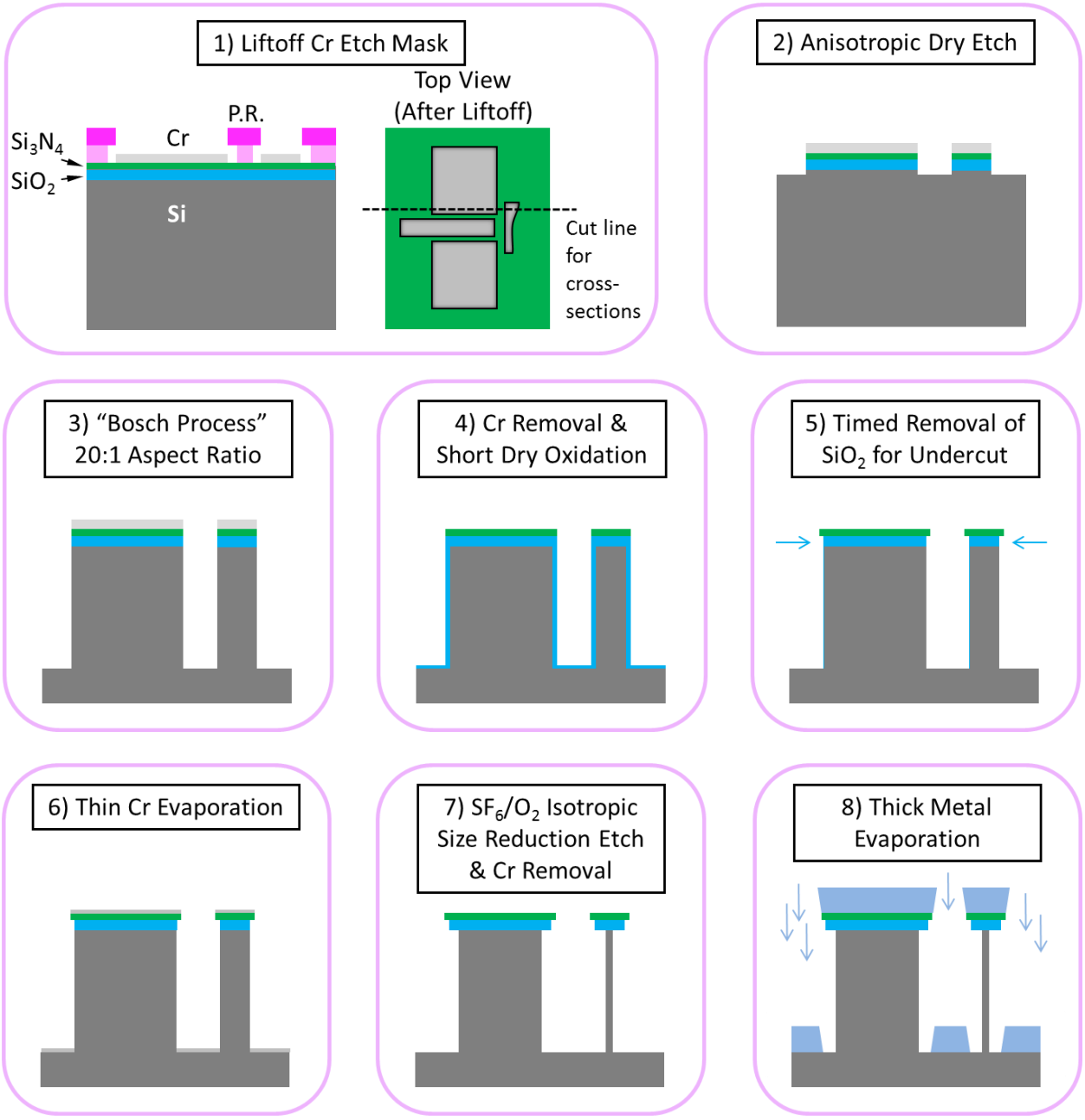
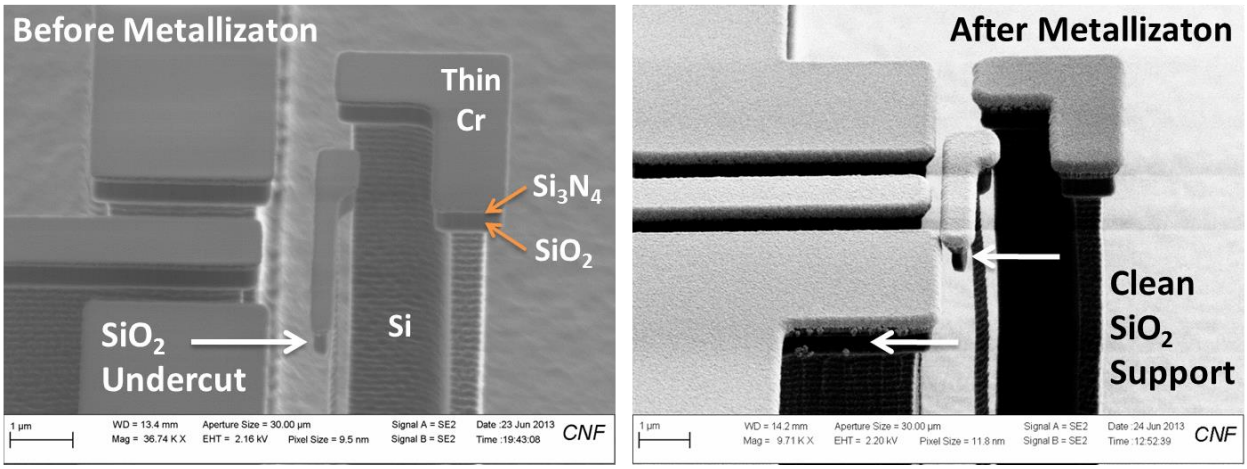


Figure 5.6: Fabrication procedure of four-terminal device without silicon nitride sidewall.



(a) **(b)**

Figure 5.7: SEM images of structure without Si_3N_4 sidewall. (a) Structure before thick metallization. SiO_2 undercut clearly visible. (b) Structure after metallization. Device in image experienced pull-in during imaging. Recessed SiO_2 appears essentially clear of metal.

Numerous devices were tested to ascertain their DC behavior. V_{DS} = 0.1 V, V_P = 0V, and current compliance was set to 1 nA. The first device had an initial turn-on voltage of ~ 17 V, as seen in Figure 5.8(a). Repeated sweeps continued to show switching behavior at a slightly higher voltage. The Gate current (I_G) can also be observed for one sweep, showing essentially no leakage during switching. Another device, one of the best in the batch, demonstrated pull-in at ~ 14.5 V (Figure 5.8(b)). The device width (pillar thickness) was drawn ~ 50 nm narrower than the device that exhibited ~ 17 V operation. Although it is somewhat difficult to characterize the thickness of the pillar given its position under the Channel, it was shown in Section 2.5.4 that devices with comparable air gaps and pillar dimensions will experience a qualitatively different electrostatic force if a sidewall (and underlying silicon) is present. Figure 2.17 showed the simulation results for a device with and without the enhanced capacitive coupling achieved from the nitride sidewall process. Devices without the nitride sidewall are expected to experience a reduced electrostatic force and higher pull-in voltage than the structures with the nitride sidewall.

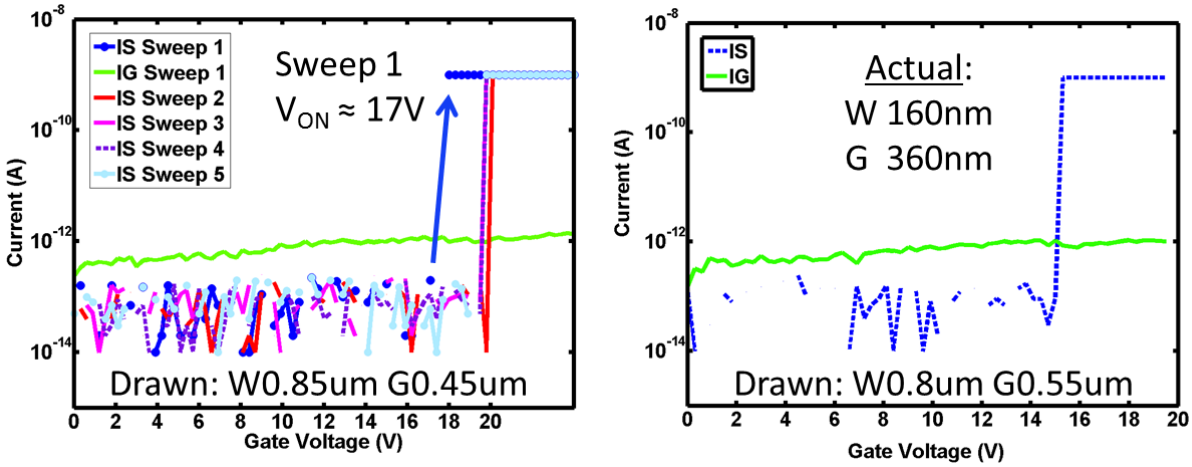


Figure 5.8: I-V plots of typical devices resulting from fabrication process without Si_3N_4 sidewall. (a) Device turns on at ~ 17 V, with repeated operation observed at a slightly higher voltage. Gate remained electrically isolated during switching. (b) Another device, with drawn width (pillar thickness) slightly narrower demonstrated pull-in at ~ 14.5 V.

5.4.2 Four-Terminal Device with Angled Sidewall

Although the vertical structure with angled sidewall strongly resembles the earlier structures with sidewalls, a few key differences exist that enable improved fabrication results. Figure 5.9 shows the fabrication procedure for the structure with angled sidewall. Starting with Step 2, a subtle difference can be observed. The anisotropic dry etch for patterning the SiO_2, Si_3N_4, and bulk silicon is stopped early, before all the planar Si_3N_4 is removed. By leaving ~ 50 nm of Si_3N_4, vertical etching in the silicon can be eliminated. Therefore, as soon as the DRIE in Step 3 clears the Si_3N_4, silicon undercut will occur. The DRIE in Step 3 is performed in the same type of ICP etcher that the cyclical BOSCH process (Step 6) uses, however, the results are quite distinct. Whereas the BOSCH process is tailored to give vertical sidewalls by cycling SF_6 and C_4F_8, the etch performed in Step 3 was implemented with simultaneous flow of SF_6 and C_4F_8. By tuning the chamber pressure and the percentage of C_4F_8 in SF_6 [126], a small and controllable undercut was achieved. It has also been shown that sidewall angle can in the

BOSCH process can be controlled in the cyclic process by modifying the flow rate of the C_4F_8. A lower flow rate results in thinner polymer deposition and a negative (reentrant) profile [127]. Additionally, the SF_6 was able to break through the remaining Si_3N_4 from Step 2. After depositing the LPCVD nitride in Step 4, a dry etch was performed to create the nitride sidewall spacers. It was unknown whether the nitride at the foot of the feature would etch in a highly anistropic process, given that it is shadowed by the top of the feature (Figure 5.10(a)). A nitride foot would result in exactly the same predicament as the vertical sidewall, with deposition occurring at the foot of the feature. Using CF_4 in an ICP etcher, it was found that the etch followed the angled profile of the sidewall to remove the nitride at the foot of the feature. Additionally, it was unknown whether the BOSCH deep etch in Step 6 would transfer the pattern in accordance with its size at the top of the feature (because of masking of the narrowed feature at the bottom), or if it would follow the size of the feature as it appears at the foot (Figure 5.10(b)). A wider silicon feature with a notch at the top (assuming the nitride foot was etched) would cause difficulty in the isotropic size reduction etch, with the silicon feature pinching off at the top of the pillar. The BOSCH etch was also found to follow the narrower feature at the bottom of the sidewall. The anisotropic CF_4 trim in Step 8 (Figure 5.9) was necessary to level the Si_3N_4 sidewall with the planar nitride to ensure proper metal deposition. Additionally, a thin Cr layer in Step 10 (Figure 5.9) was used to protect the top nitride surface from the SF_6/O_2 etch in Step 10. Finally, a thick metal was deposited on the structure. The results were as desired. Thin pillars, clean sidewalls, and small air gaps were achieved without sacrificing the electrical or mechanical properties of the device.

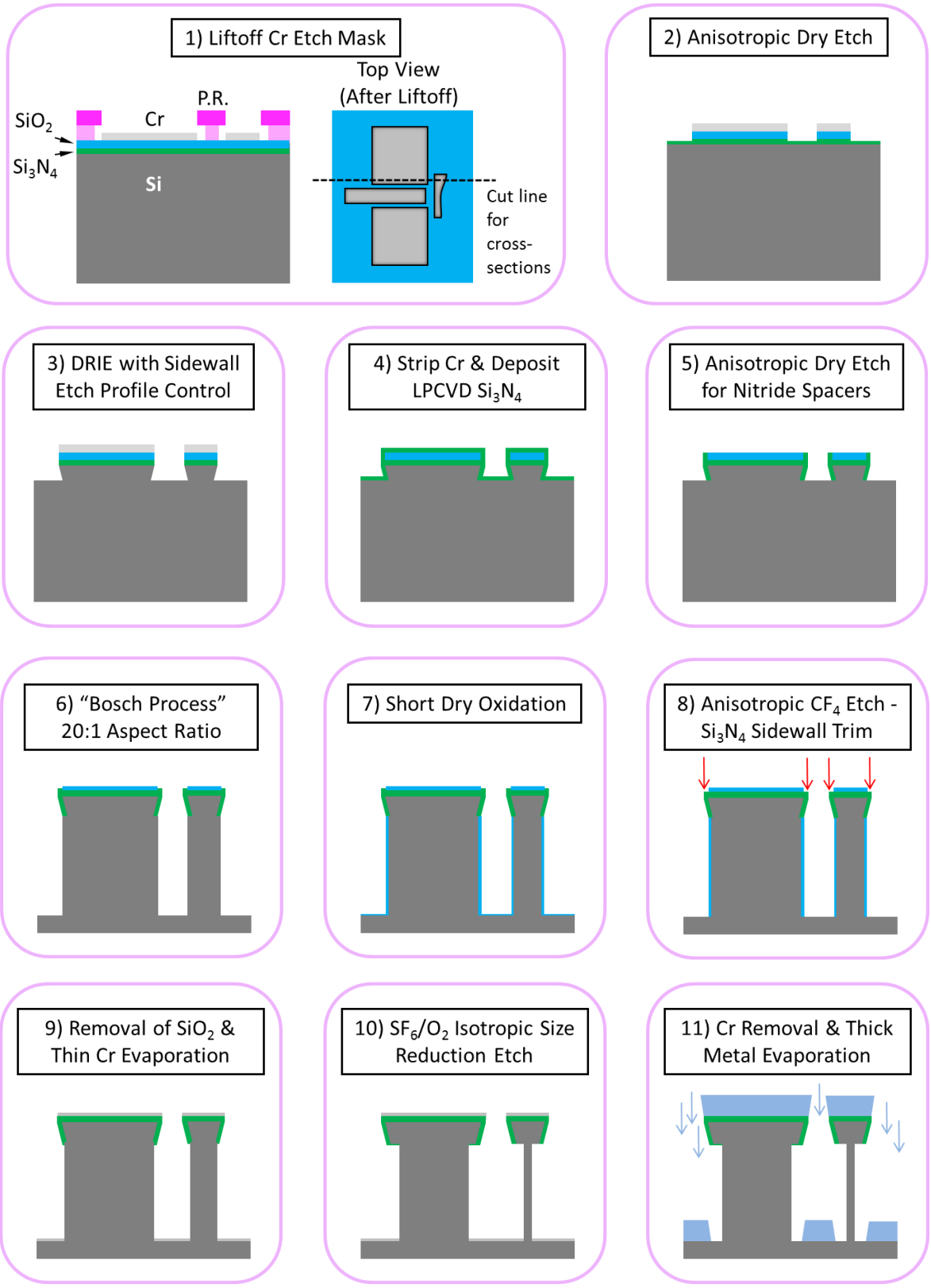


Figure 5.9: Fabrication procedure for four-terminal device with angled silicon nitride sidewall.

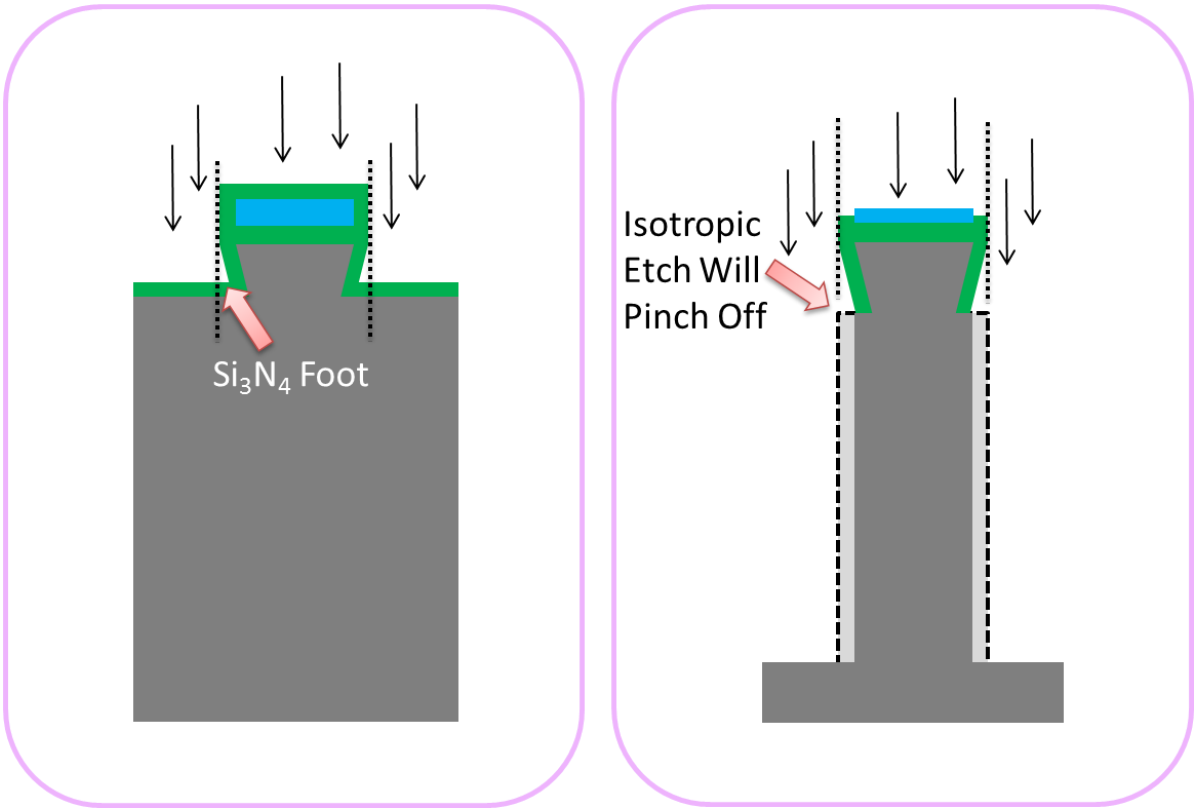


Figure 5.10: Potential challenges for anistropic etching when features have angled sidewalls. Dotted lines represent etch profile of highly anisotropic etch. (a) Dry etch for nitride spacers could result in Si_3N_4 foot because of shadowing from top of feature. This would inevitably result in metal deposition on an undesirable location. (b) Deep etch could result in wider feature with notch at top. Subsequent isotropic etch for size reduction would pinch off the pillar at the top.

The results of the top-down four-terminal fabrication procedure with angled sidewall can be seen in Figure 5.11. The sloped etch profile is significant and perceptible without cross-sectioning the device. After the final metallization, extremely clean nitride sidewalls were achieved, even in narrow regions of the device. The thick metal evaporation substantially reduced the air gap size, as can be seen by the angle of the metal deposition. The silicon nanopillar, as seen in Figure 5.11(c), can also be seen to be clean of metal. One slightly undesirable feature can be noticed. The top of the nanopillar is narrow than the bottom. This pillar profile can result in stiffer structures.

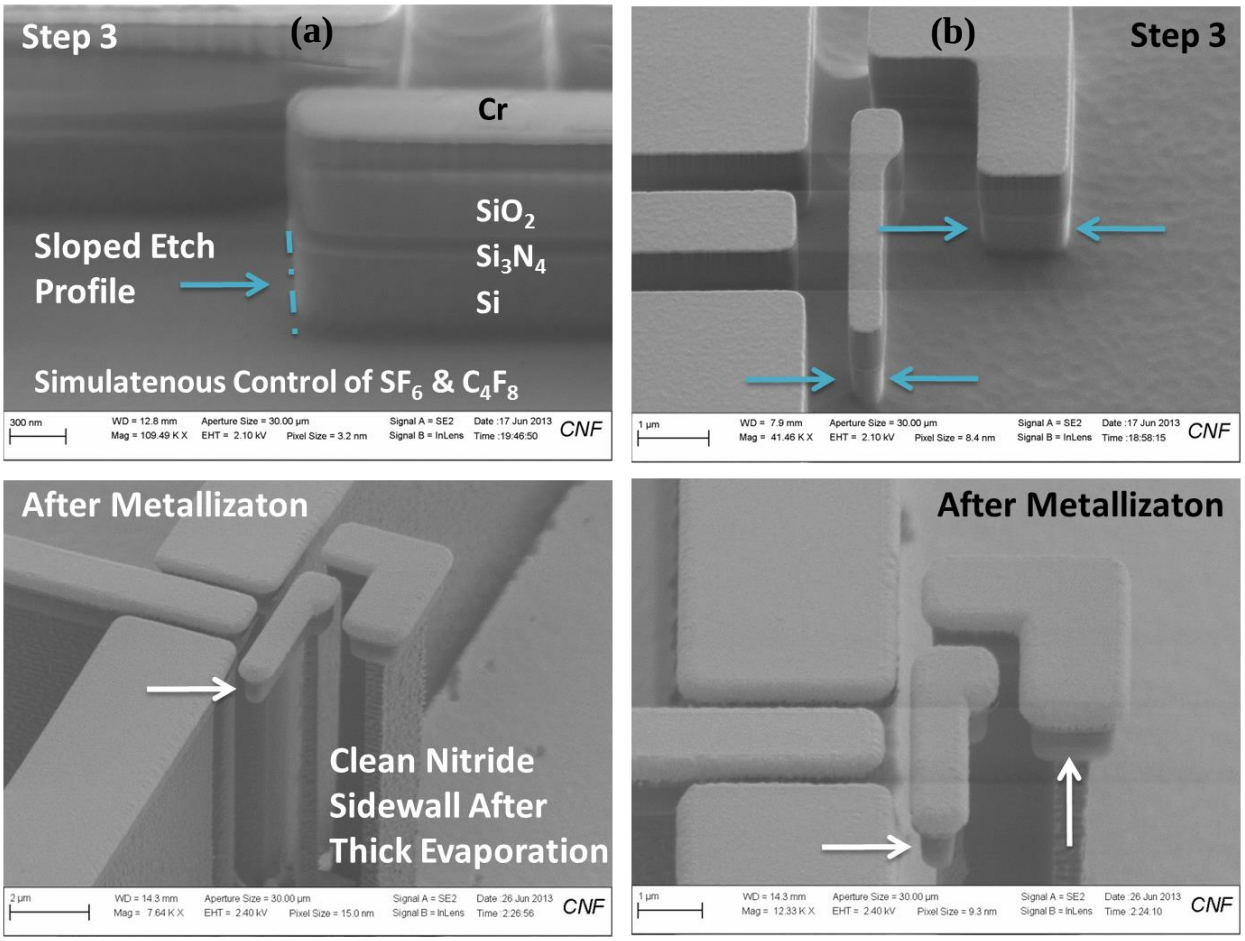


Figure 5.11: Fabrication results for four-terminal top down device with angled sidewall. (a) SEM image facing the Channel after Step 3 (Figure 5.9). SF_6 and C_4F_8 are used simultaneously to control the etch profile. (b) SEM image of side view of device. Angle of silicon walls is quite noticeable. In narrow region between S/D/G and Channel, silicon etch is more shallow. (c) Three quarters view of completed device after metallization. Nitride sidewalls are completely clear from metal deposition. (d) Side view of completed device. Narrow region between electrodes is clear from metal and suitable for abrupt switching behavior.

The electrical results of the top-down four-terminal devices with angled sidewalls were consistently good. The testing conditions were the same as those for the devices without sidewall: V_{DS} = 0.1 V, V_P = 0V, and a current compliance of 1 nA. A number of devices exhibited reproducible switching. Figure 5.12 shows a device that initially switched at ~ 13.5 V. By sweeping forward and reverse, it was possible to observe pull-out of the switch at ~ 2 V. A

low pull-out voltage (large hysteresis) can be the result of strong surface adhesion forces as well as the electrostatic force (previously discussed in Section 1.3.2.1). Repeated sweeps demonstrated consistent switching at a lower voltage, ~ 10 V.

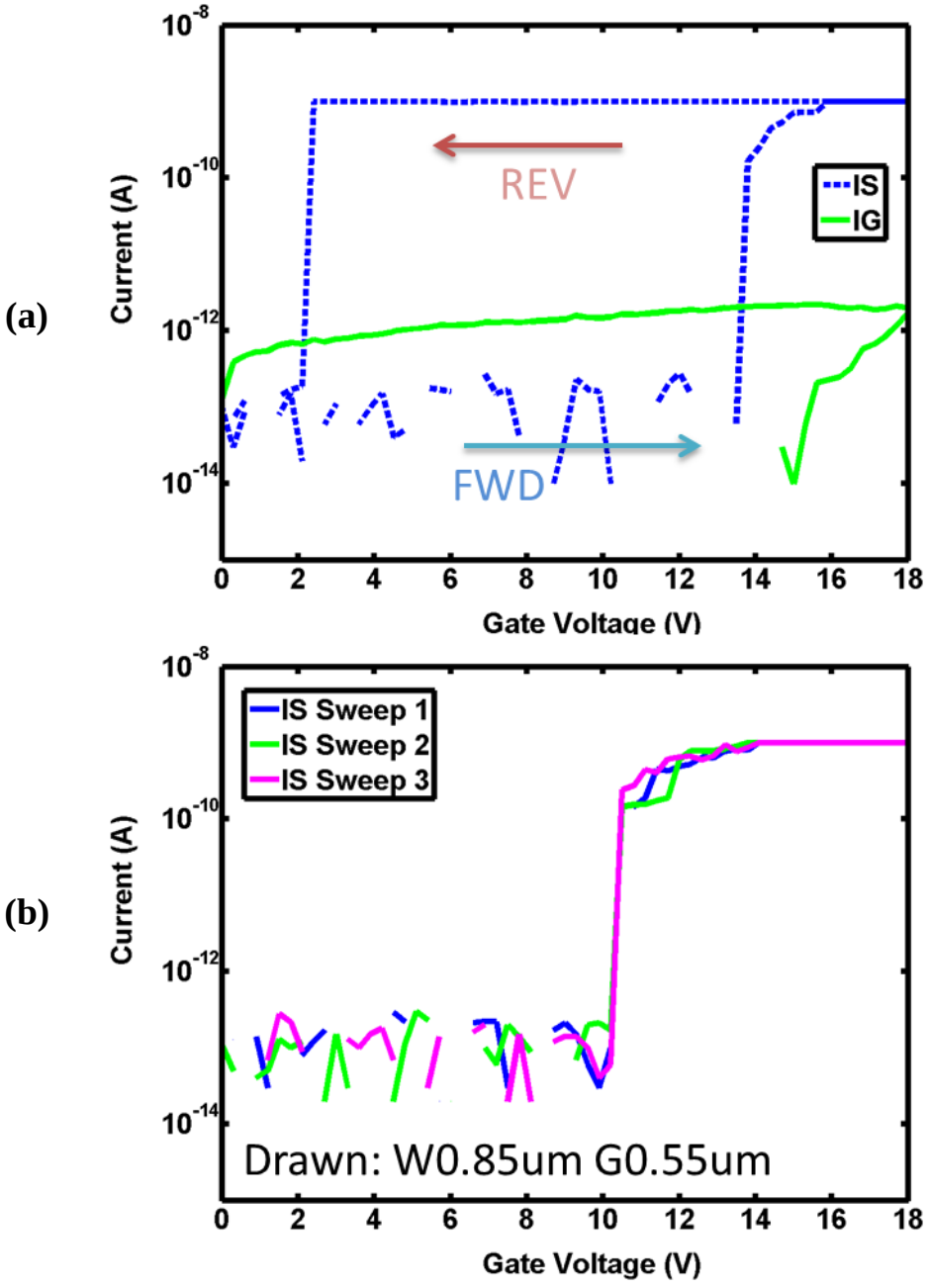


Figure 5.12: I-V plots of a single device fabricated using the angled sidewall process. (a) Initial pull-in occurred at ~ 13.5 V. By sweeping forward and reverse, pull-out was observed at ~ 2V. (b) Repeated sweeps of the same device show consistent switching at a lower voltage, ~ 10 V.

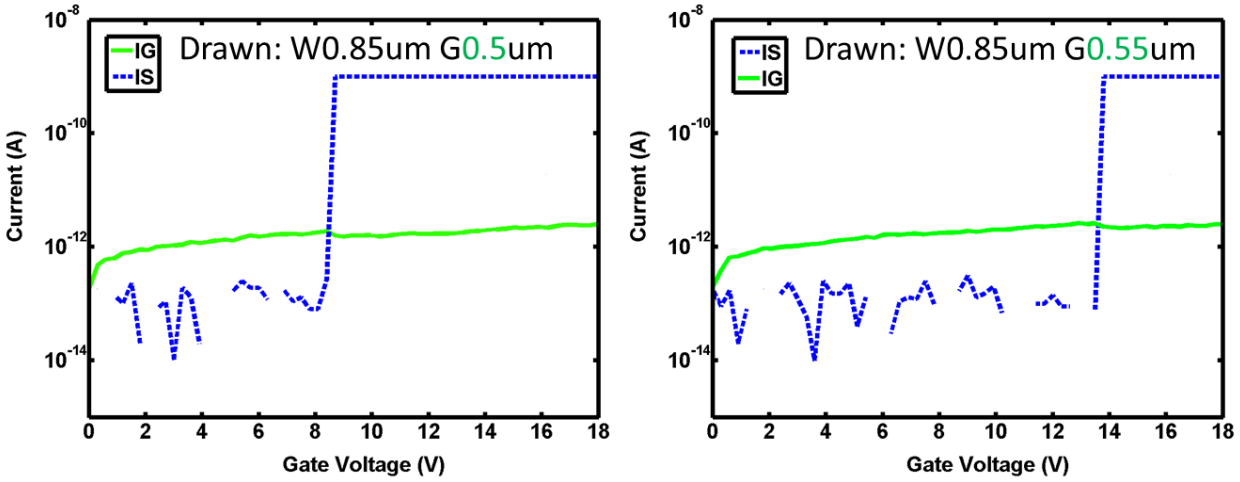


Figure 5.13: I-V plots of typical devices fabricated with the angled sidewall process. (a) A low voltage switch exhibiting a pull-in voltage of ~ 8 V. (b) Another device of similar dimensions with slightly large drawn gap. Pull-in achieved at ~ 13.5 V, similar to the device in Figure 5.12.

Other devices of interest can be seen in Figure 5.13. A particularly low voltage switch can be observed in Figure 5.13(a). Pull-in voltage was measured at ~ 8 V for the device. Additionally, another device of similar drawn dimensions, with slightly large air gap (0.55 µm vs. 0.5 µm, before metallization) demonstrated pull-in at ~ 13.5 V. The device in Figure 5.13(b) has the same drawn dimensions as the device in Figure 5.12, and both demonstrated initial pull-in at ~ 13.5. After measuring numerous devices with and without the nitride sidewall, it was seen that the devices with the angled sidewall generally exhibited lower pull-in voltages. Both fabrication processes resulted in more working devices from batch to batch. However, the fabrication process without sidewall typically resulted in more working devices due to the simplicity of the process. Chips with working devices from both fabrication techniques were used to conduct the 3D NEMS integration experiment.

5.5 NEMS BONDING DESIGN

The NEMS bonding experiment was designed to test the feasibility of bonding and electrically contacting freestanding (released) nanoscale structures without using planarization or dispersion of liquids in (or before) the bonding process. Wet processing of NEMS devices poses a potential risk to device integrity. The fabrication processes developed in this thesis have not used any wet processes once the nanopillars have been isotropically etched to their final dimensions. Unlike planar devices which invariably require a release step (from the substrate) that is typically wet, the vertical structure is freestanding from the time the nanopillar is patterned in the middle of the process flow. Therefore, the ideal 3D bonding process would retain the benefits of dry processing during all the back-end handling. This work proposes and demonstrates a process suitable for bonding large arrays of nanomechanical devices while maintaining air gaps around the devices so as to allow movement of the mechanical structures during operation.

The specific bonding process was chosen in accordance with the discussion in Section 5.2 regarding the bonding techniques that result in electrical conductivity between the bonded structures. The potential methods include metal thermocompression, eutectic, and transient liquid phase bonding [118][128]. Considering the current generation of vertical nano-relays have gold metallization, CMOS contamination was also not one of the criteria for choosing the bonding materials. Bonding materials were chosen primarily based on considerations of thermal budget and ability to bond structures with topography and surface roughness. Eutectic and transient liquid phase bonding tolerate some surface roughness and particle contamination as a result of their transition into the liquid phase during bonding. While in the liquid (soft) phase, the bonding material can reflow around particles to incorporate them or fill nanoscale voids from

roughness. This is assuming the particles and roughness are on the same size scale as the bonding layer thickness.

Initially the NEMS bonding experiment was to be performed in a full wafer bonder under vacuum. However, due to alignment difficulties with chip to wafer bonding, the experiment was moved to a flip chip bonder. Given the constraints of the bonder and the availability of metal sources capable of bonding to the gold device electrodes, indium was chosen as the intermediate bonding layer between the chip and wafer. Pure indium can be easily thermally evaporated to form bumps through a lift-off process. Figure 5.14 shows the intended 3D integration scheme with CMOS and NEMS switches. Metal bumps deposited or patterned on the CMOS layer serve to connect the CMOS with the individual NEMS device electrodes. The height of the bump and the extent to which it compresses during bonding will determine the cavity height (air gap) above the Channel/nanopillar structure. For this bonding experiment, a simplified approach is taken, similar to the work performed by IBM (Figure 5.4). A "dummy CMOS" layer consisting of metal lines on a borofloat wafer is bonded to a NEMS device array using indium bumps, as depicted in Figure 5.15.

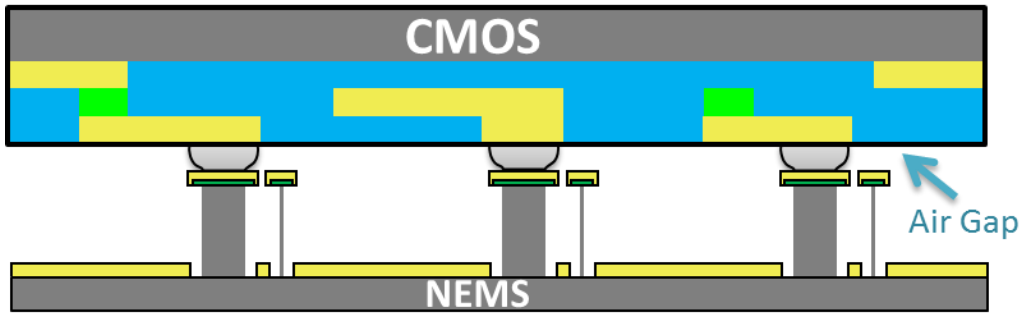


Figure 5.14: Schematic of 3D integration of CMOS and NEMS with metal bumps as intermediate layer. Metal bumps determine cavity height (air gap) of CMOS layer up the Channel/nanopillar.

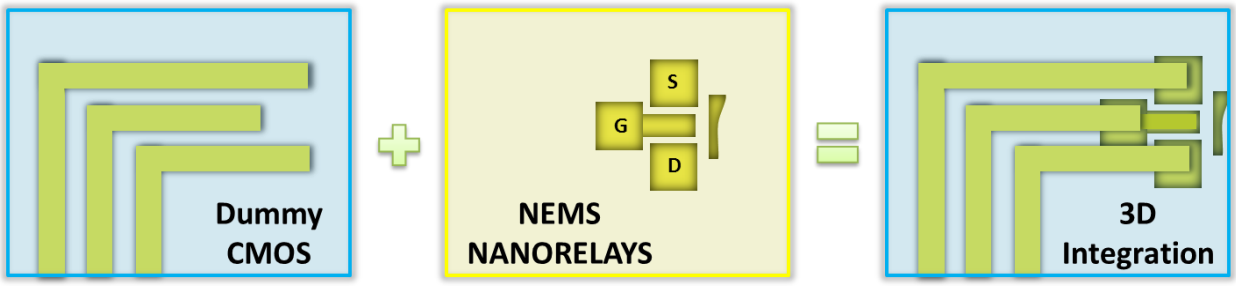


Figure 5.15: Simplified 3D integration scheme with dummy CMOS (metal lines on a borofloat wafer) bonded to NEMS nanorelay array. Indium bumps are evaporated directly onto the dummy CMOS wafer.

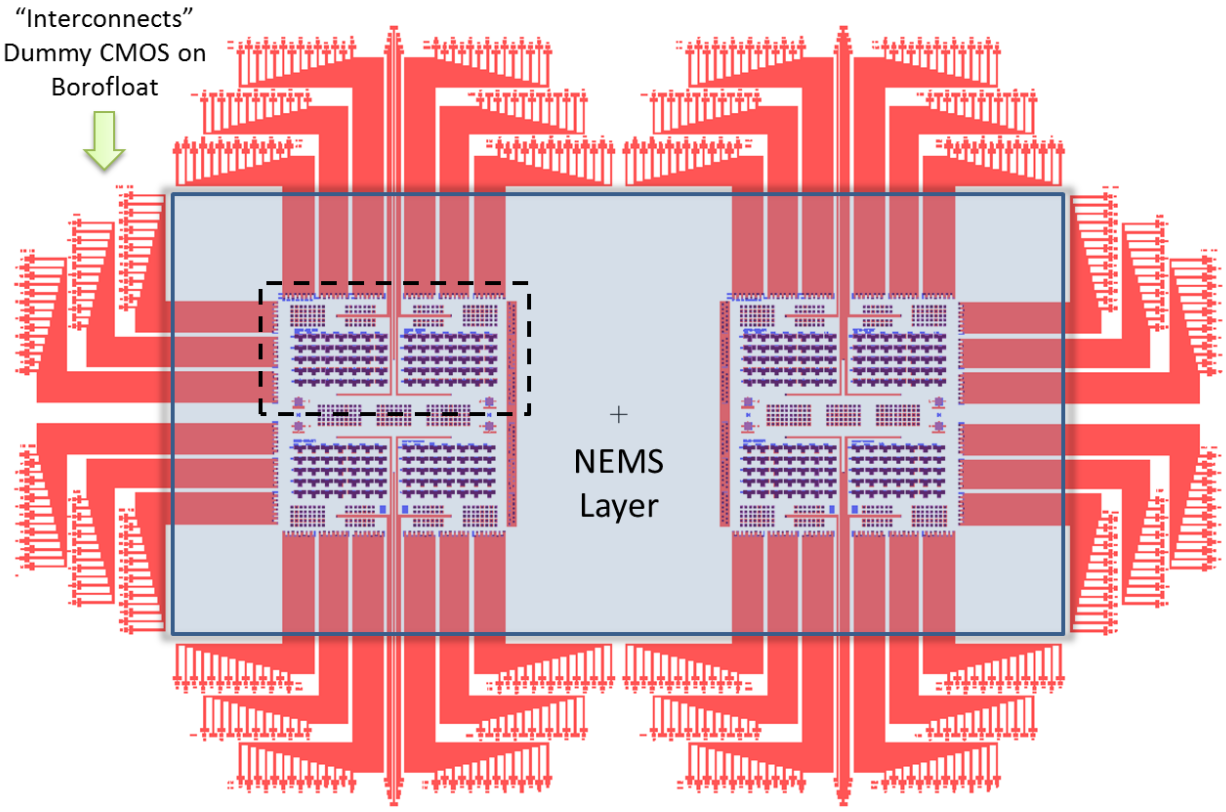


Figure 5.16: CAD layout of 3D integration mask set. 3 masks are shown (overlayed), 2 for the dummy CMOS, and 1 for the NEMS device layer. The large rectangle represents a silicon NEMS chip with two dies for bonding (for use with the full wafer bonder). The small dashed rectangle represents the actual NEMS chip bonded by the flip chip bonder (requires smaller pieces). The "interconnects" are gold lines deposited on the borofloat wafer. They are used to access and measure the devices that are bonded.

The 3D NEMS integration mask set is shown in Figure 5.16. Borofloat is chosen for the CMOS dummy wafer to enable easy through-wafer alignment (transparent substrate) and non-invasive post-bonding optical verification of alignment and condition of test structures. The mask was originally designed for bonding two NEMS dies on a single chip with two point alignment to the dummy CMOS wafer. The large shaded rectangle represents the NEMS chip with two dies. The small dashed rectangle represents a cleaved portion of the chip. A smaller chip was required for flip chip bonding. The image contains three masks that are overlayed. One mask is used to create the gold "interconnects" for measuring the bonding devices. Gold lines are patterned using liftoff of Cr and Au, 10 nm and 80 nm respectively. The bonded devices are enclosed between the silicon NEMS chip and the borofloat wafer. The gold "interconnects" run along the surface of the borofloat wafer beyond the extents of the NEMS chip to enable access to the bonded devices. A second mask is used for patterning the indium bumps located at the end of the gold lines. The indium bumps are patterned using liftoff. A thick liftoff resist of ~ 3.5 – 4 μm is spun on the borofloat wafer. Approximately 3.5 μm of indium were evaporated on the dummy CMOS wafer at a rate of ~ 7 – 9 Å/s. The evaporation rate should be kept preferably lower than these rates to prevent substrate heating and reflow of indium bumps during evaporation.

NEMS devices with small pads were located at the peripheral of the NEMS chip. These devices are used for characterizing switch operation post –bonding. The pads on the peripheral NEMS devices are 17 μm x 17 μm. The gold lines on the dummy CMOS wafer are 20 μm wide. Additionally, the indium bumps for bonding of the small peripheral devices are ~ 10 μm x 10 μm. Therefore, the NEMS device pads have ± 3.5 μm alignment tolerances for the indium bumps on the dummy CMOS wafer. NEMS devices with larger pads are located in the center of

the mask. They are used to characterize the devices in the pre-bonding condition, as done in Section 5.4. Also, two terminal resistance test structures are included throughout the mask design to characterize the indium to gold bond resistance. Figure 5.18 shows images of the fabricated samples for use with the 3D NEMS integration experiment. Figure 5.18(a) shows the size of a peripheral NEMS device that is specifically designed for post-bonding testing. The indium bumps for bonding can be seen in Figure 5.19(b). The bumps exhibit a large amount of roughness (~ 100's of nanometers) as deposited. This roughness is undesirable for bonding.

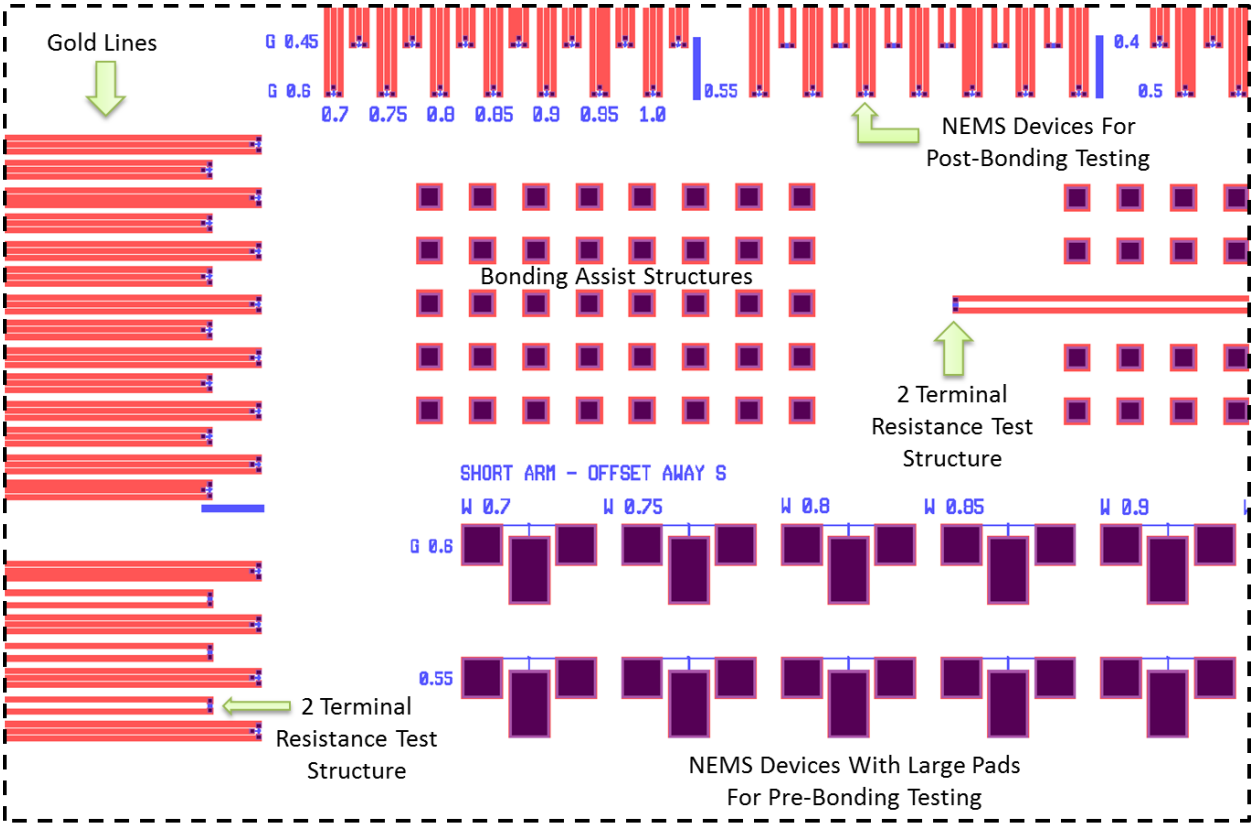
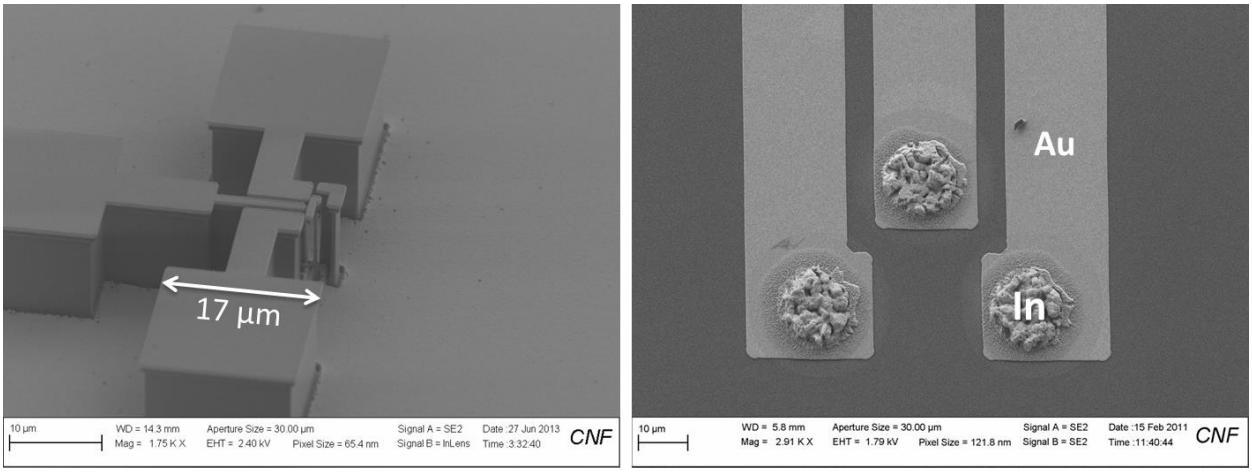


Figure 5.17: Enlarged view of portion of 3D NEMS integration mask set. NEMS devices for post-bonding testing are at the peripheral of the chip. NEMS devices with large pads for pre-bonding testing (with probe-station) are in the center of the chip. Two terminal resistance test structures are dispersed throughout the mask. Bonding assist structures fill empty space, add contact area for bonding, and help distribute the force uniformly from the bonder.



(a) **(b)**

Figure 5.18: SEM images of fabricated 3D NEMS integration samples. (a) Peripheral NEMS switch with small bonding pads. (b) Gold lines on borofloat. Indium bumps patterned by liftoff at the end of the gold lines.

5.6 BONDING RESULTS

Bonding was performed on a Finetech flip chip bonder. The top chip picker, as seen in Figure 5.19, has a small area of 3 mm x 5 mm. It uses vacuum to hold the top substrate; however, no heating for the top substrate was available for the configured tool model. The bottom substrate simply rests on the heated chuck without any vacuum. The heated chuck can accommodate a larger sample of ~ 50 mm x 50 mm. However, due to the small size of the chip picker, the NEMS chip must be cleaved to a reasonable size, as depicted by the dashed rectangle in Figure 5.16. A top chip that is much larger than the chip picker will not experience uniform pressure during bonding if the chip picker only presses on the center of the chip. The tool has a specification of one micron resolution. The flip chip bonder uses a stationary monocular view to image the top and bottom substrates via a beam splitter. These images can be overlayed for

alignment, as seen in Figure 5.19(b). A stationary monocular view makes rotational alignment quite challenging while only using the features in the field of view for reference.

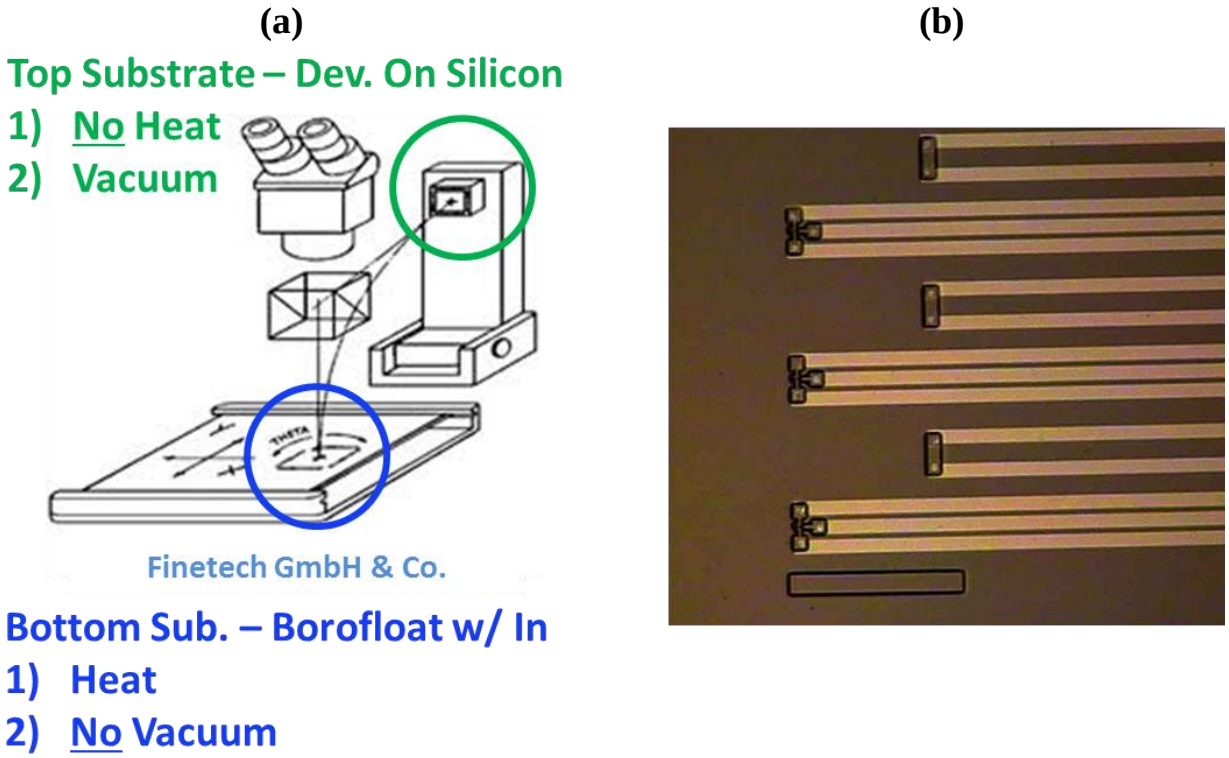


Figure 5.19: Flip chip bonder configuration. (a) Top substrate (NEMS chip) is held by vacuum on vertical arm. Bottom substrate (dummy CMOS with indium) rests on heated chuck. (b) Image seen through flip chip optics. Stationary monocular view with split-view of top and bottom samples overlayed for alignment.

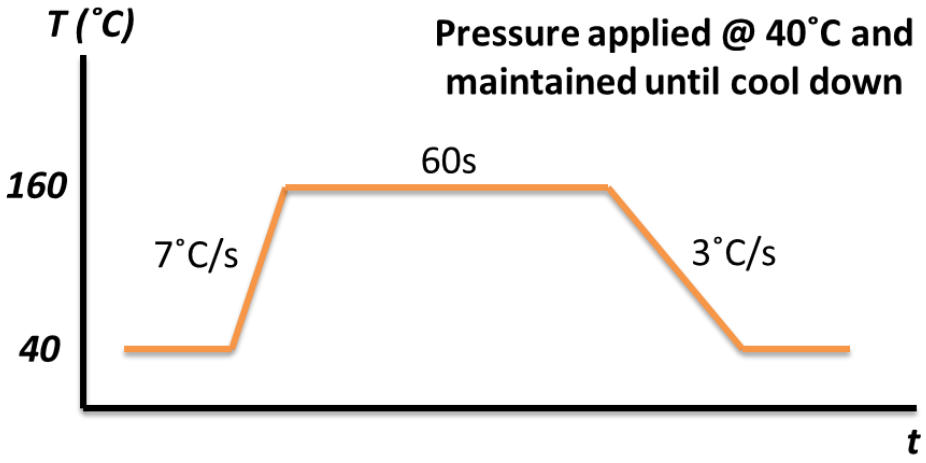
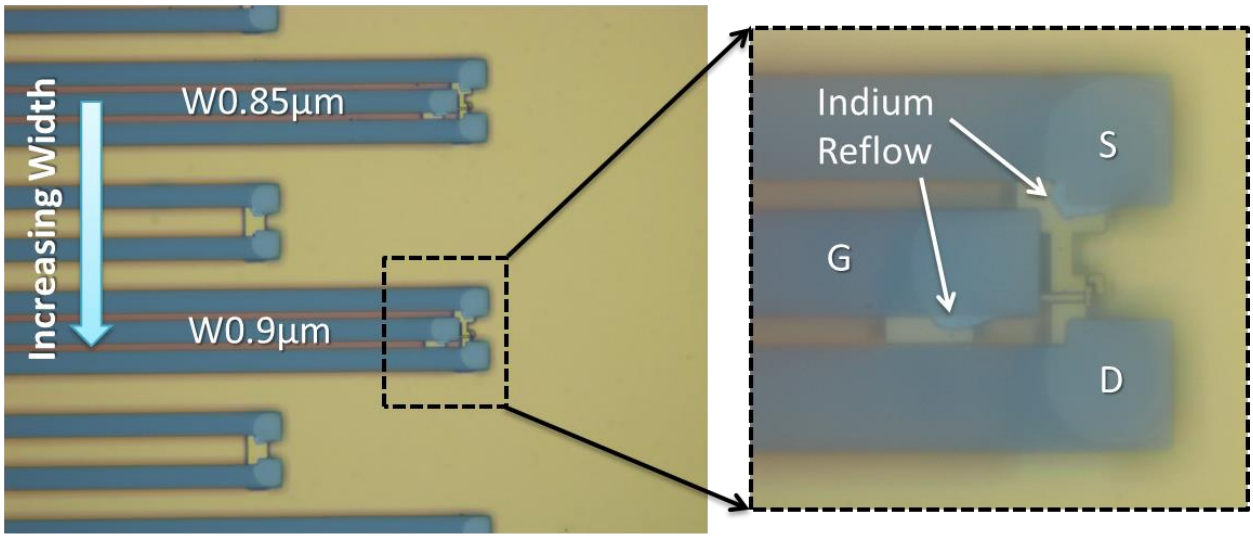


Figure 5.20: Flip chip bonder heating profile for bottom substrate during bonding.

After conducting a number of experiments for bonding temperature, it was found that the optimal bonding temperature for evaporated indium bumps on a glass (borofloat) substrate is ~ 160 ˚C (melting temperature of indium). For higher temperature the indium easily reflows and wets the gold surface, thereby lowering the average height of the indium bump. Figure 5.20 shows the flip chip bonder heating profile used for bonding. Pressure must be maintained on the samples until the temperature returns to ~ 40 ˚C to ensure that the substrates remain in contact while the indium is cooling. A manual lever weight system is used to set the force during bonding. The applied force was in the 10's of newtons.

The first sample to show successful bonding of the NEMS nanorelays to the dummy CMOS can be seen in Figure 5.21. Images with an optical microscrope are captured while looking through the backside of the borofloat wafer. The gold lines (interconnects) appear grey as a result of the chrome adhesion layer that was used for the gold liftoff process. A column of devices at the perimeter of the bonded chip are imaged in Figure 5.21(a). The mask layout for the NEMS switches consisted of rows or columns of devices with constant air gap size and increasing Channel width size (in 50 nm increments). Figure 5.21(b) shows an enlarged view of a device that is successfully bonded with a few microns of misalignment in the x- and y-directions. Indium reflow is also apparent at the edge of the gold lines on the borofloat wafer. This reflow is most likely the result of excessive pressure during bonding. Although it visually appears that the Gate "interconnect" is contacting the Source electrode on the device, the electrical data does not indicate such a condition. Therefore, it is unlikely that there is any indium on the top right corner of the Gate "interconnect" to short to the Source. Electrical characterization was performed on this device. The same testing conditions were used as previous measurements: V_{DS} = 0.1 V, V_P = 0V, and a current compliance of 1 nA. For a vertical

structure with angled sidewall, and drawn dimensions of width 0.9 µm and gap 0.55 µm, pull-in was observed at ~ 17.5 V, as seen in Figure 5.22. Repeated operation was also observed. Additionally, no gate leakage was detected in the bonded device. If pressure during bonding resulted in any damage to the thin silicon nitride layer in the device, more gate leakage would be expected during measurement, which was not the case. Another bonded sample can be observed in Figure 5.23. This sample has NEMS devices without the sidewall. Figure 5.23 (b) and (c) are images of two neighboring devices after electrical characterization. The first device, having drawn width of 0.85 µm, exhibits no current. The second device, having drawn width of 0.9 µm, exhibits some conduction, although it appears to be from the Source to the Gate. It is quite common for Source and Gate terminals to short during operation (via the Channel) if the Gate – Source offset is not sufficiently large. Images of the two devices appear significantly different. An enlarged view of the first device appears to still have a gap, whereas the second device does not appear so. Figure 5.24(a) shows the electrical data for the bonded switch in Figure 5.23(c). Additionally, Figure 5.24(b) shows the conduction through a two terminal resistance test structure located between the two devices of interest, as seen in Figure 5.23. A low resistance path is seen between the two gold lines, thereby confirming that bonding has succeeded in that region. Extracted resistance of the two Au – In bonds is ~ 357 Ω. Therefore, a single bond is ~ 178 Ω. Other resistance test structures showed even lower resistance. These values for resistance are also quite small in comparison to the resistance of the current generation of NEMS switches. Overall, the bonding experiment demonstrated the ability to make a number of chip-to-chip electrical contacts in a small area (3 bonds per switch). Furthermore, the bonding process revealed the resilience of the devices during bonding and their proper operation post-bonding. Macroscale images of the bonded chips can be seen in Figure 5.25.



(a) **(b)**

Figure 5.21: Optical verification of 3D bonding with NEMS devices seen through borofloat wafer. (a) A column of devices at the perimeter of the bonded chips. Devices have identical drawn gap sizes and increasing values for width. (b) Enlarged view of bonded structure. Indium reflow apparent at the edge of the gold lines on the borofloat sample. Misalignment quite noticeable.

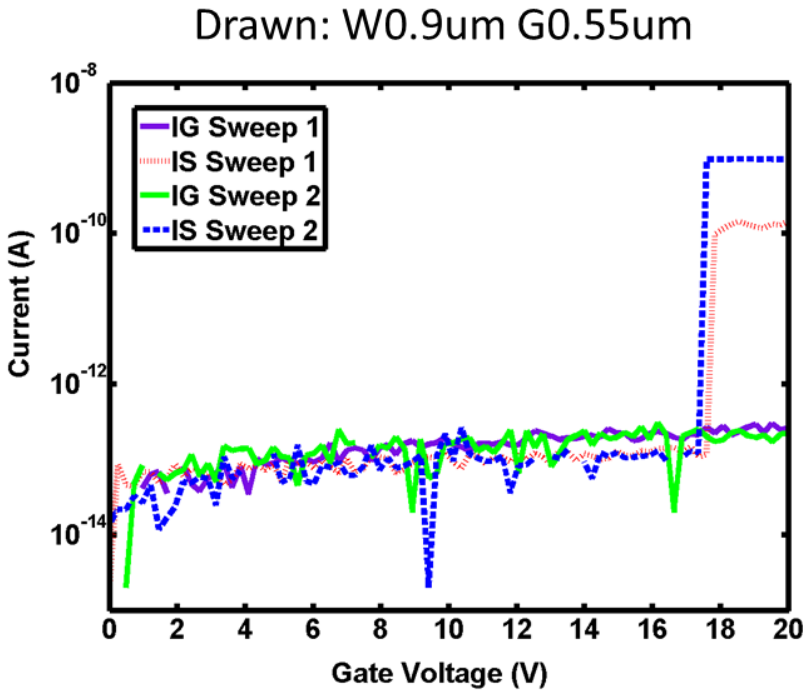


Figure 5.22: Electrical data of bonded NEMS structure (with angled sidewall) measured via the gold "interconnects" on the dummy CMOS chip. No gate leakage present. Device exhibits pull-in at ~ 17.5 V and repeated operation.

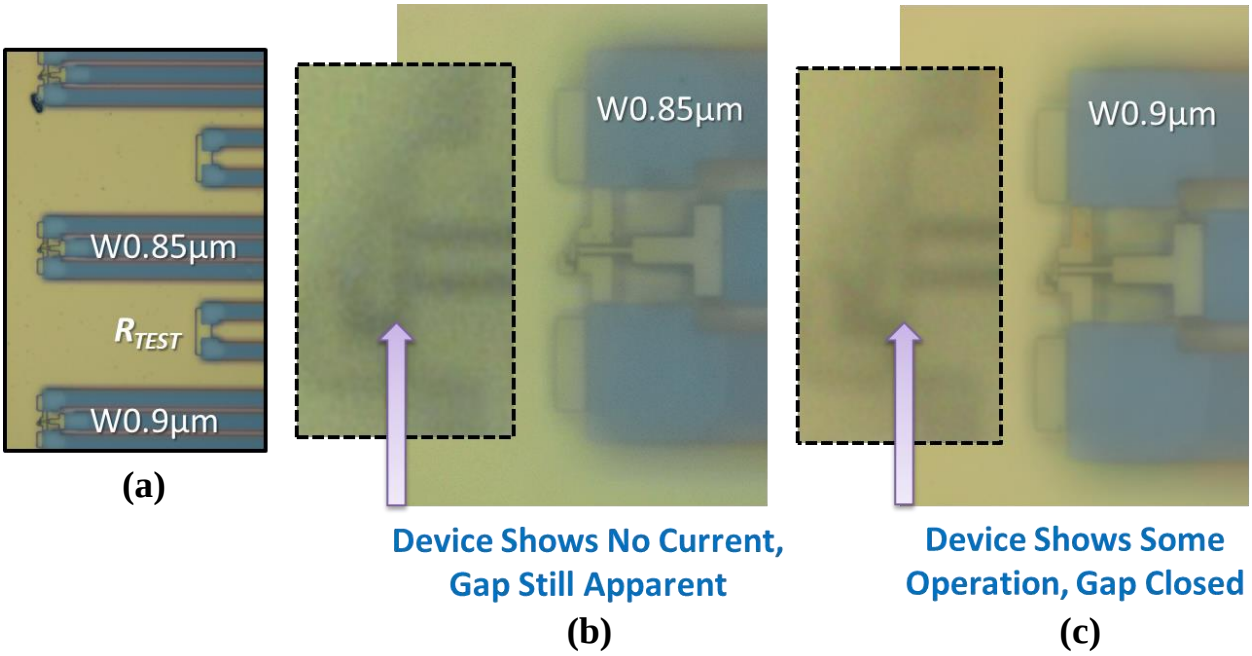


Figure 5.23: Optical verification of NEMS device characteristics for devices without sidewall. (a) A column of devices with constant air gap size on peripheral of chip. R_{TEST} is two terminal resistance test structure. (b) Image of device having drawn width of 0.85 µm. No current observed. Enlarged view in dashed rectangle. Gap still visible. (c) Image of device having drawn width of 0.9 µm. Some operation observed. Enlarged view in dashed rectangle. Gap appears closed.

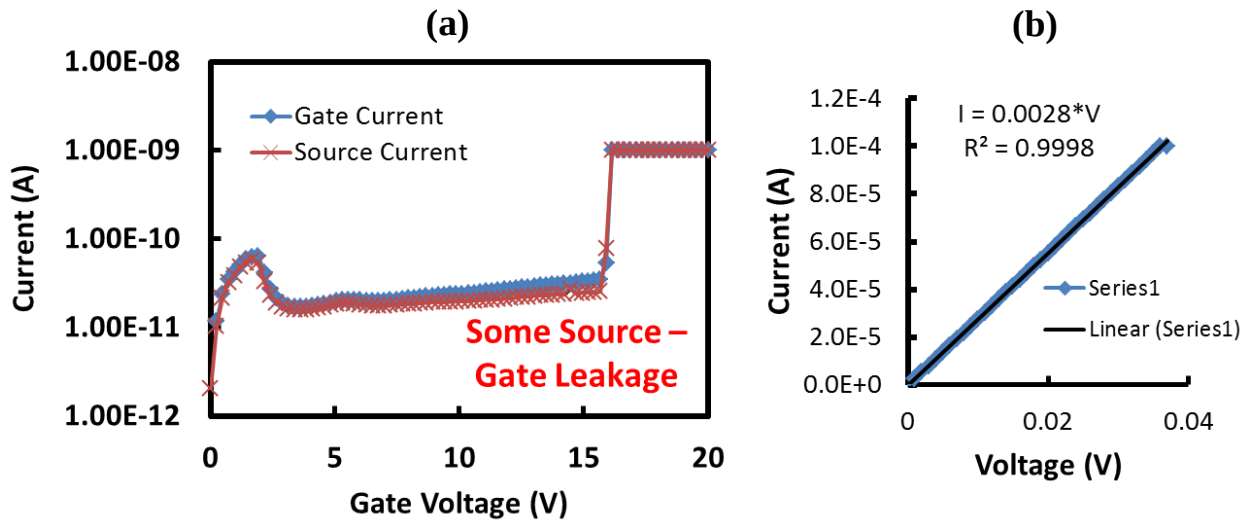
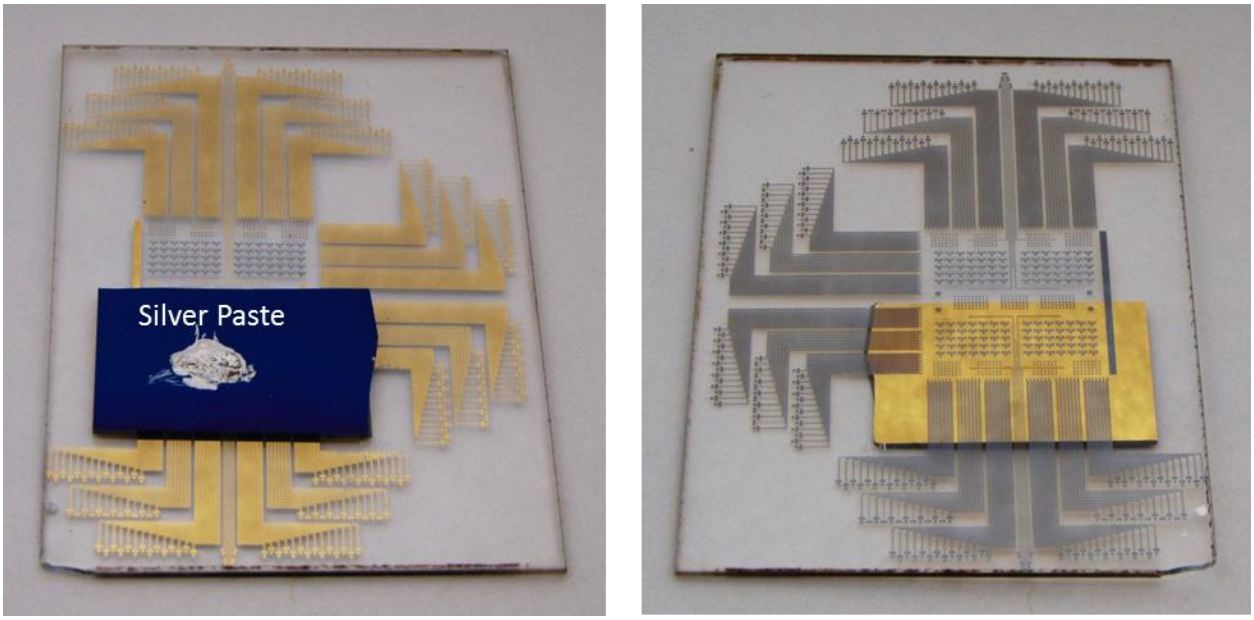


Figure 5.24: Electrical data of bonded NEMS structure without sidewall measured via the gold "interconnects" on the dummy CMOS chip. (a) Device with drawn gap of 0.9 µm. Although Source current is detectable, it appears Source is connected to the Gate. (b) Extraction of Au – In bond resistance from two terminal resistance test structure.



(a) **(b)**

Figure 5.25: Macroscale images of bonded NEMS chip to dummy CMOS wafer. Chips contain half the mask design of Figure 5.16 to enable flip chip bonding. Borofloat wafer is diced using CO_2 IR laser. (a) Dummy CMOS chip (borofloat with gold lines) on bottom, and NEMS chip on top. Silver paste on NEMS chip is used for making pillar/substrate contact. (b) Image of bonded sample looking through the backside of the dummy CMOS wafer.

5.7 ISSUES

A number of formidable issues arose during the bonding experiment. Since each peripheral group of devices has a constant value for air gap and increasing values for Channel width, it is only expected that one or two devices in each group will operate within a reasonable range of voltages. For smaller widths the devices are pulled-in during fabrication, and for larger widths the operation voltage is very large. Furthermore, different groups of devices have different values for air gap size, and only certain values produce working devices. Gaps that are too small are filled by metal during evaporation, and gaps that are too large result in devices with very high operation voltages. Therefore, it is expected that only a small number of the devices

on the peripheral of the chip will be of interest. However, it was unexpected that the device operation of the peripheral devices would differ significantly from the center devices with large pads. Pre-bond characterization was performed on the center devices, where numerous working devices were found. During the bonding experiment, although a number of device appeared to be successfully bonded, very few showed proper switching behavior. It was not possible to easily probe the peripheral devices before bonding to ascertain their device characteristics. The other main difficulty was with the bonding apparatus itself. Since the flip chip bonder uses only a single stationary objective to perform alignment, rotational alignment was particularly challenging. Furthermore, the field of view was not able to capture the entire sample. Consequently, only a small region of the chip was in alignment during the bonding process. All these factors combined to result in very few measurable and working devices post-bonding. With no vacuum on the bottom chip and the chip picker too small for the NEMS chip (top substrate) shifting of samples and non-uniform force distribution both occurred during bonding. Therefore, a much more rigorous bonding apparatus is necessary to perform a thorough investigation of NEMS bonding.

CHAPTER 6

CONCLUSIONS & FUTURE WORK

6.1 CONCLUSIONS

Fundamental difficulties in CMOS scaling have resulted in increased exploration of alternative and complementary approaches to computing. This dissertation has investigated NEMS switches as a potential candidate for integration with CMOS. NEMS switches have attractive qualities that can help curb the increase in power density seen by CMOS scaling. Nanomechanical switches offer essentially zero subthreshold swing (abrupt switching) and no off-state leakage. Leakage is suppressed by using nanoscale air gaps for isolation and switching operation controlled by physical contact of a moveable element. Numerous varieties of MEMS/NEMS switches exist in many different manifestations. Almost all devices are of a planar orientation. However, when considering compact device designs, a vertical structure that does not occupy much silicon real-estate will lead to ultimate scalability. Additionally, practical device considerations were discussed, and emphasis was placed on the need for multi-terminal structures for simple circuit implementation. Designs with a minimum of three terminals, and ideally four terminals are best suited for NEMS switches. This thesis proposes and demonstrates a new class of devices that takes account of these design considerations. The work herein sets forth the first multi-terminal top-down vertical NEMS switch.

Numerous fundamental challenges also exist for creating multi-terminal top-down nanoscale switches. The design and fabrication of three terminal and four terminal devices was discussed in detail. A design based on an electrically floating Channel is best suited for top-down vertical implementations. Channel potential is controlled by capacitive voltage division.

It was also found that a combination of torsion and bending is necessary for reproducible switching in nanoscale devices exhibiting levels of roughness common to lithography and metallization. Using a nanopillar based structure capable of both modes of motion, 10 V operation was observed for a device with an air gap of ~ 230 nm and a non-uniform pillar thickness of ~ 130 – 180 nm. Uniform scaling of all dimensions indicates sub – 1 V operation for a factor of 10 size reduction. Additionally, improvements to the single step lithography process were made throughout a number of iterations. Devices with an angled silicon nitride sidewall were shown to have good device characteristics and decoupling of the mechanical and electrical design parameters.

Although the four terminal device behaves more like a three terminal device after initial pull-in (due to bending), this design opens the door to more advanced top-down vertical structures. Limitations in speed (as compared to CMOS) and reliability suggest that NEMS switches are best suited for enhancement of CMOS functionality and performance, as opposed to outright replacement. However, materials restrictions and thermal constraints of CMOS fabrication indicate that heterogeneous integration will be practically achieved via 3D chip bonding technology. This dissertation demonstrated a simple bonding technique useful for NEMS – CMOS integration. Programming was achieved by means of bonded electrical interconnects, and nanoscale vertical devices were shown to endure the bonding process. This process demonstrates the potential for integration of large and dense arrays of nanomechanical switches with CMOS. A higher resolution bonding apparatus along with materials better suited for nanoscale bonding will be required for practical implementations. Cu – Cu bonding has shown promising results for preliminary experiments with MEMS – CMOS integration [129]. Use with a vertical structure will potentially require a means for depositing Cu on the bond pads

and not the NEMS switch. Tighter constraints for roughness and flatness will also be required for interesting bonding techniques such as Cu – Cu room temperature bonding, capable of sub-micron alignment [115]. As device scaling continues, 3D (vertical) devices, structures, and integration schemes will continue to be of greater interest and value. The new class of vertical structures developed in this dissertation will potentially lead to many alternate compact vertical structures in addition to low voltage NEMS switches.

6.2 FUTURE WORK: A TRUE FOUR-TERMINAL VERTICAL SWITCH

Although a four terminal vertical structure was discussed in Chapter 4, it was noted that the operation of the switch resembles that of a three terminal structure after the Channel is in physical contact with either the Source or the Drain. Upon contact, the Channel potential is determined by the Source/Drain potential and not the capacitive voltage divider. Furthermore, before the device is pulled-in, since the potential of the Channel is determined by a capacitive voltage divider, some of the Gate voltage is dropped across the fixed Si_3N_4 capacitor beneath the Channel. Therefore, this mode of operation requires a larger voltage than a simple parallel plate configuration. In order to create a more scalable device that has a well-defined pull-in voltage (independent of the Source/Drain voltages) a new structure must be suggested. The structure must still utilize torsion and bending to overcome nanoscale difficulties for contact switches. Figure 6.1 shows an improved structure for an ultra-low voltage NEMS top-down four-terminal vertical switch. A large vertical electrode (Gate) runs parallel to the Pillar/Body electrode. These electrodes form a simple parallel plate actuator with gap defined by thin film growth or deposition. The Channel is once again used to connect the Source and Drain electrodes. However, the Gate has been relocated and is no longer between the Source and Drain, as seen in

Figure 6.2. In this new configuration, the Channel does not play a significant role in the electrostatics, and only goes for a ride as a result of the Gate/Pillar actuation. The Source/Drain to Channel air gap must be smaller than the Gate to Pillar air gap to ensure that contact will be made only between the Source/Drain and Channel, thereby preventing the Pillar from shorting to the Gate. The partially wrapped around vertical Gate electrode is contacted via the planar Gate electrode (which is connected to the vertical Gate by a metal layer that wraps around the device and cannot be shown in the figure).

Figure 6.2 shows a key feature of the device operation. The device should be designed such that the Drain has a fixed offset from the Source. By making the Drain – Channel gap smaller than the Source – Channel gap, the Channel will make contact with the Drain first when the pull-in voltage for bending operation is applied. At that point a small gap will still exist between the Source and Channel, as defined by the mask design. Torsion-based operation will then cause the small gap to close, thereby forming a conduction path between the Source and Drain. Since the Gate and Pillar are located towards the Source-side of the device, if the Drain electrode does not have an offset, the Channel can contact the Source electrode first, thus preventing the device from generating a torque on the Pillar via the Gate electrode.

A number of other key design features are incorporated in this device. Firstly, the vertical Gate electrode must be significantly stiffer than the Pillar. This is necessary to prevent the Gate from deflecting during electrostatic operation. Another important aspect is that the electrostatic coupling to the Pillar is potentially much stronger than the coupling to the Channel (in the original device). Since the area for capacitive coupling to the Pillar (as defined by the height) is larger than the area of coupling to the Channel, the electrostatic force is enhanced in the new design. This improvement can result in two advantages. The device can operate at

lower voltages. Or more importantly, the device can made stiffer and still operate at the same voltage as the original design. As electromechanical devices scale down, increased mechanical stiffness will greatly assist the device in overcoming the surface adhesive forces that effect contact based devices. Figure 6.3 shows a hypothetical fabrication process that can be used to create this novel structure. Although the process only uses two lithographic steps, fabrication complexity substantially increases. However, this device can be of great interest given its unique strengths and potential for ultra-low voltage switching in a compact vertical design.

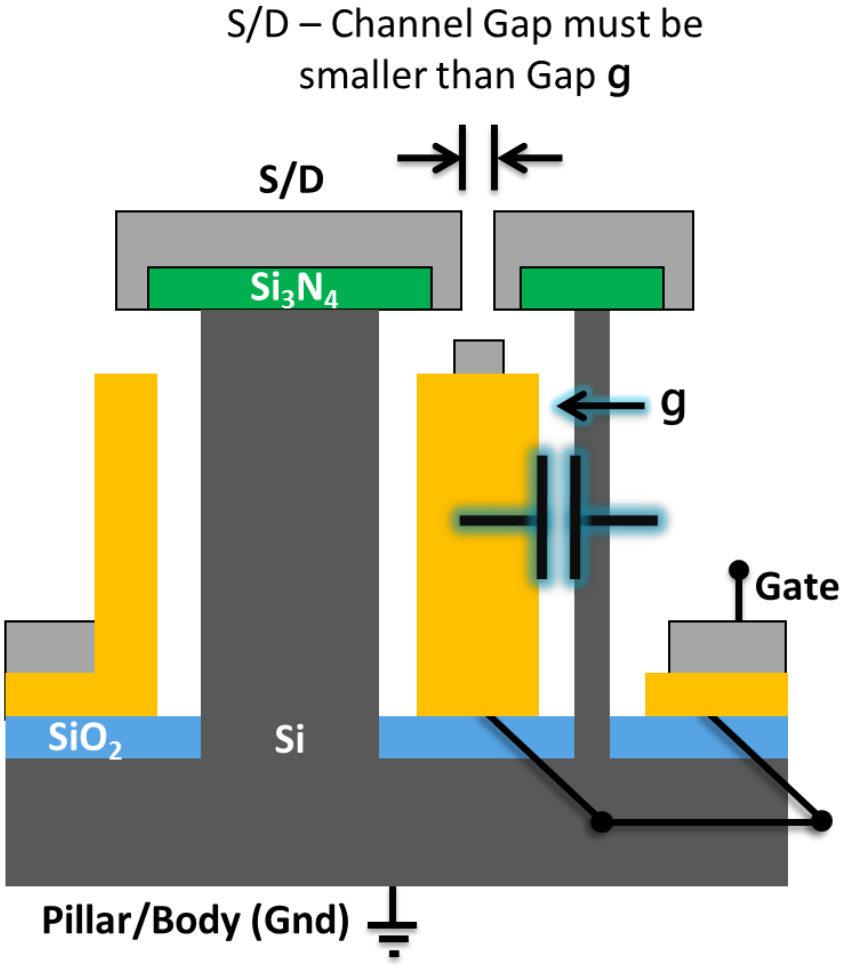


Figure 6.1: Schematic of true four-terminal top-down vertical device (not to scale). Gate electrode on substrate is connected out-of-plane to vertical gate (next to pillar). Substrate is used to ground the Pillar/Body. Moveable Channel is used to connect Source and Drain electrodes at top of structure.

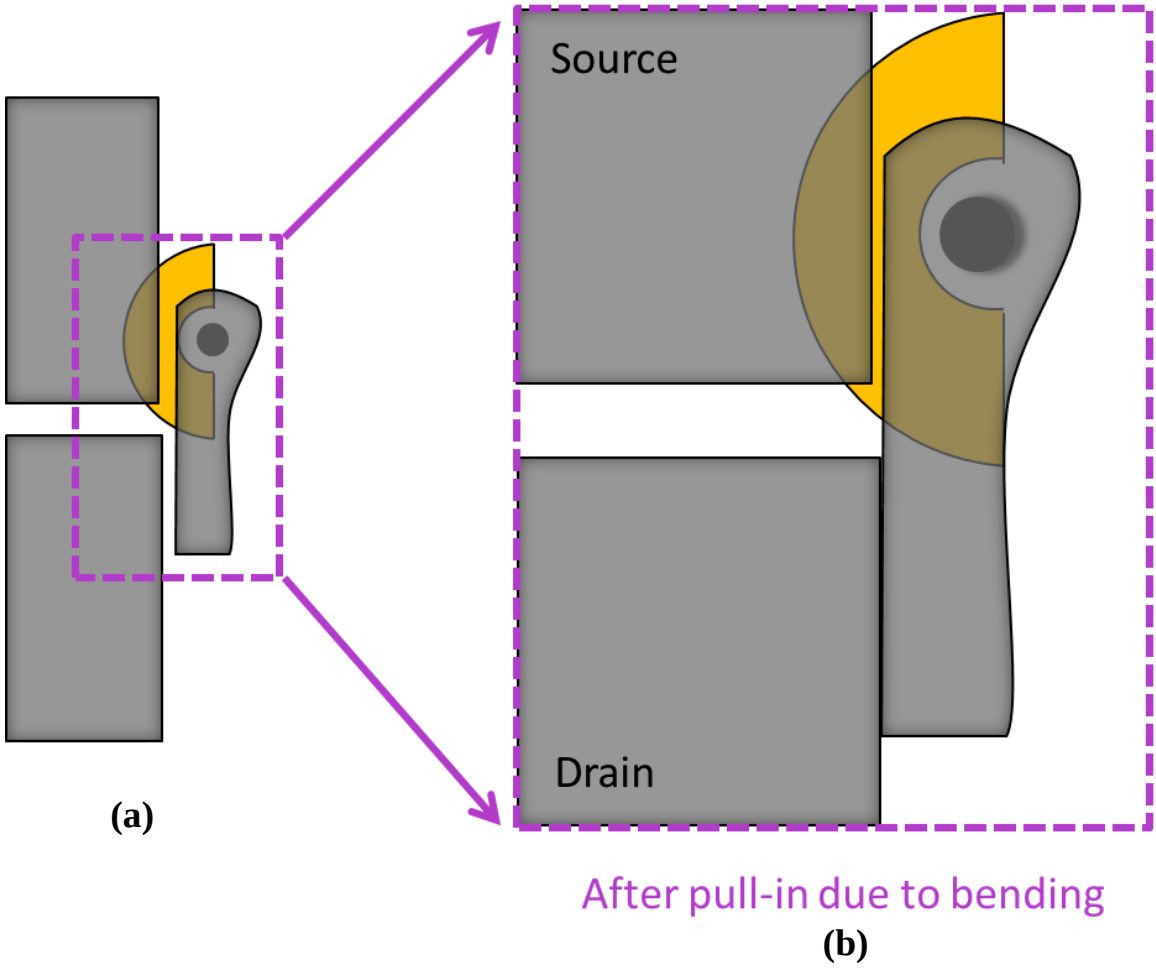


Figure 6.2: Schematic of top view of enhanced four-terminal top-down vertical device. (a) Device before pull-in. Partially wrapped around gate used to pull-in Channel/Pillar. The Drain electrode is designed to have a small offset towards the Channel with respect to the Source. (a) Device after initial pull-in (due to bending). Channel contacts Drain electrode first. Small gap remains between the Source and Channel (according to the designed offset). Additional electrostatic actuation between the Gate and Pillar will cause torsion, thereby enabling the Channel to also contact the Source.

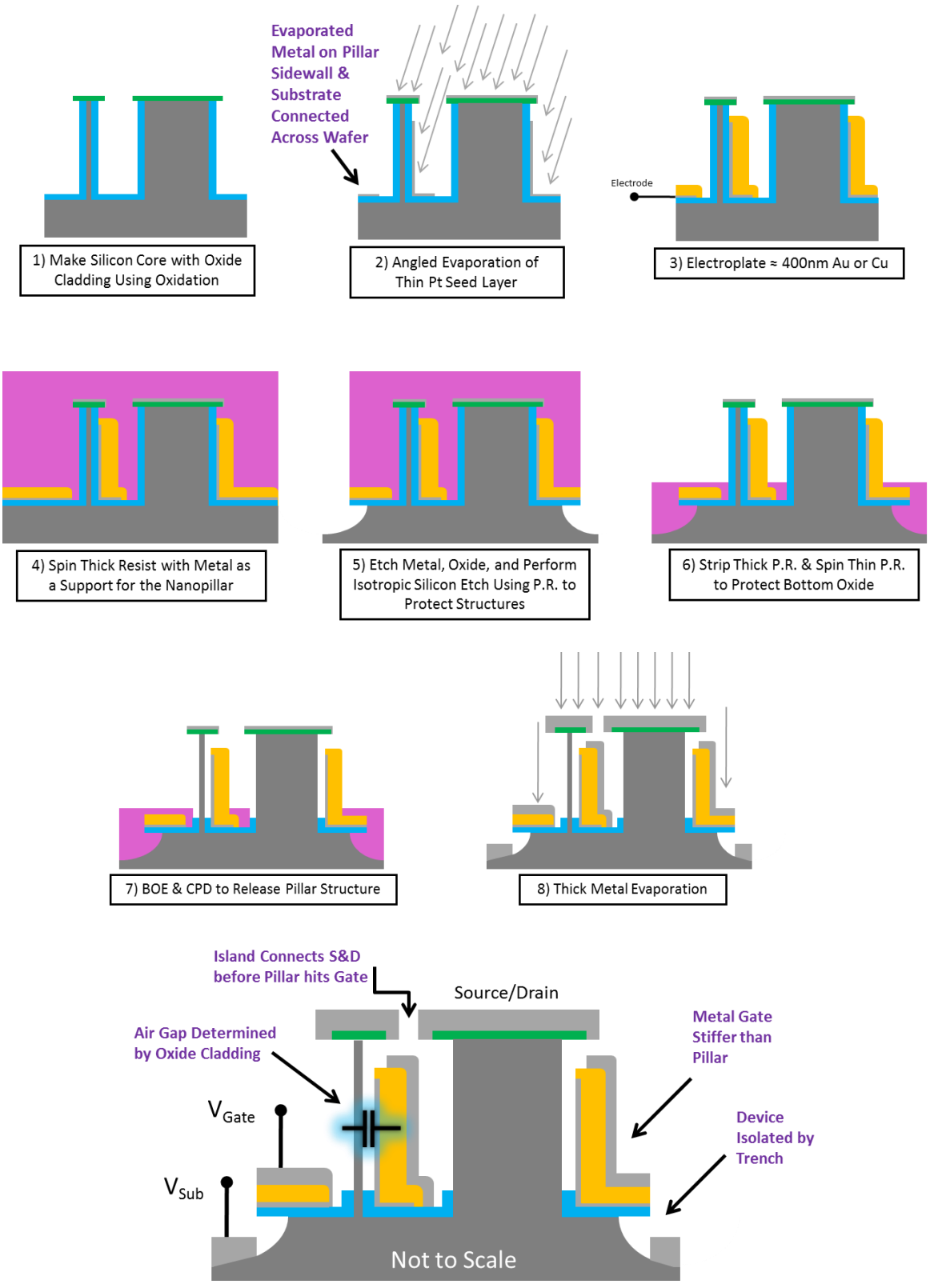


Figure 6.3: Suggested fabrication process for enhanced four-terminal top-down vertical structure. Final structure shows particular design considerations.

6.3 ENERGY HARVESTING

A popular method of converting mechanical vibrations into electrical energy is to use a capacitive energy harvester. This technique requires an external DC voltage source to charge the plates so that a change in capacitance will results in an alternating current $\left(i = \frac{d}{dt}(CV)\right)$. Additionally, the approach needs a dedicated circuit for plate charging. Considering the required overhead, Kuehne suggested using a two metal solution to eliminate the DC supply and extra circuitry [130]. Using two materials of different work-function, a contact voltage (built-in voltage) can be generated when the materials are electrically connected, as seen in Figure 6.4(b). Therefore, capacitive energy harvesting can be achieved without requiring external elements. A change in the gap between the plates will result in a transient current.

To generate a significant and useful amount of power for operating electronic devices, generally numerous energy harvesting devices will be required. The simplest and easiest approach is to connect the energy harvesting devices in parallel. However, this approach does not work for typical capacitive energy harvesters. When individual energy harvesters are driven by uncorrelated vibration sources, generated currents will cancel each other for large arrays of devices connected in parallel, as seen in Figure 6.4(d). Therefore, Ardanuc proposed and demonstrated a charge shuttle based energy harvester using two materials of different work-function [131][132], as shown in Figure 6.5. The design uses physical contact between metals of different work-function to transfer charge onto an electrically isolated charge shuttle, thereby eliminating the drawbacks of purely capacitive-based operation. A macroscale model was built using steel balls as charge shuttles, as shown in Figure 6.5. Figure 6.6 shows the electrical results for the macroscale model. As the number of balls in parallel increases, the output power

rapidly increases. The preliminary results suggest that a micro- or nano-scale version with vast arrays of charge shuttles can be of great interest.

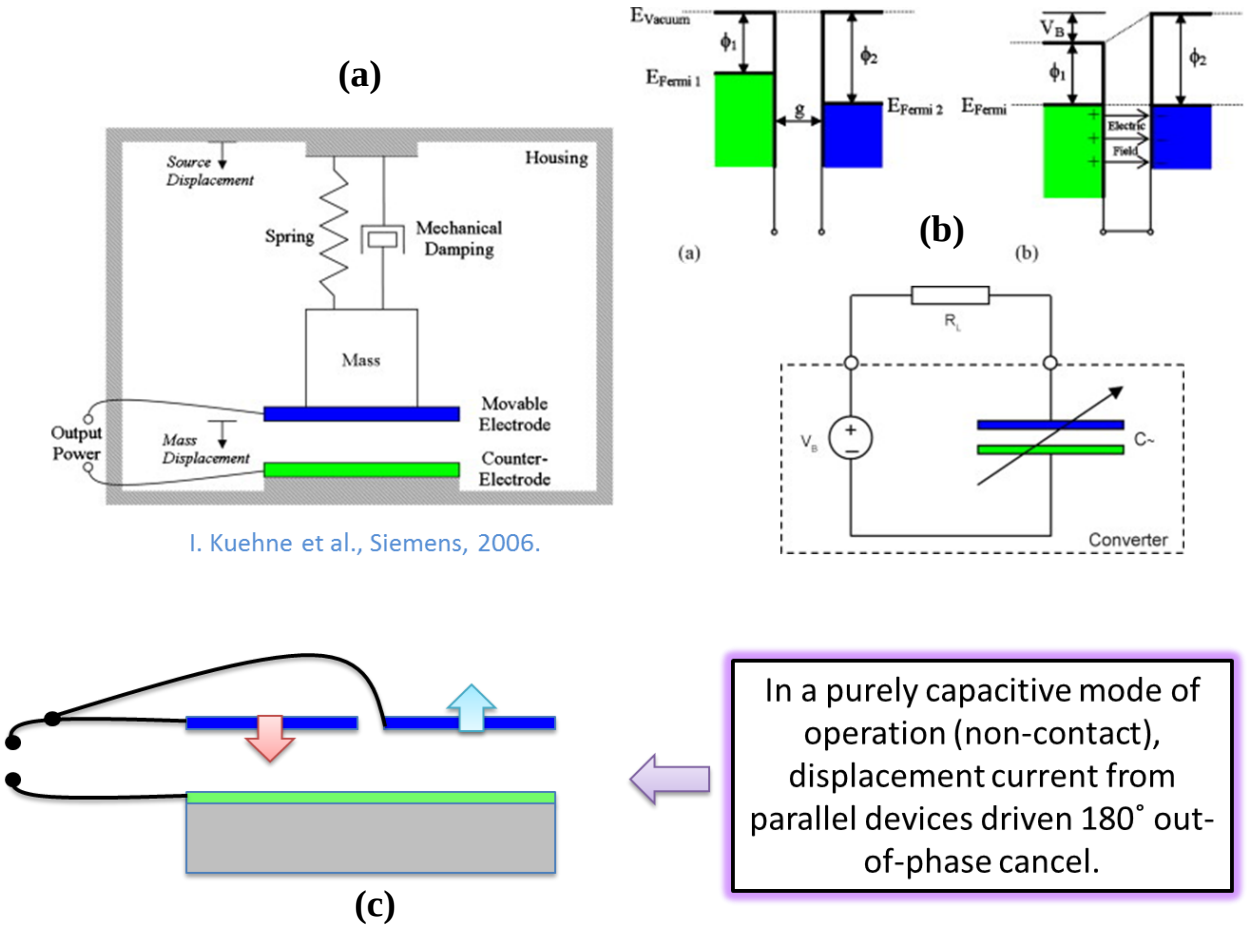
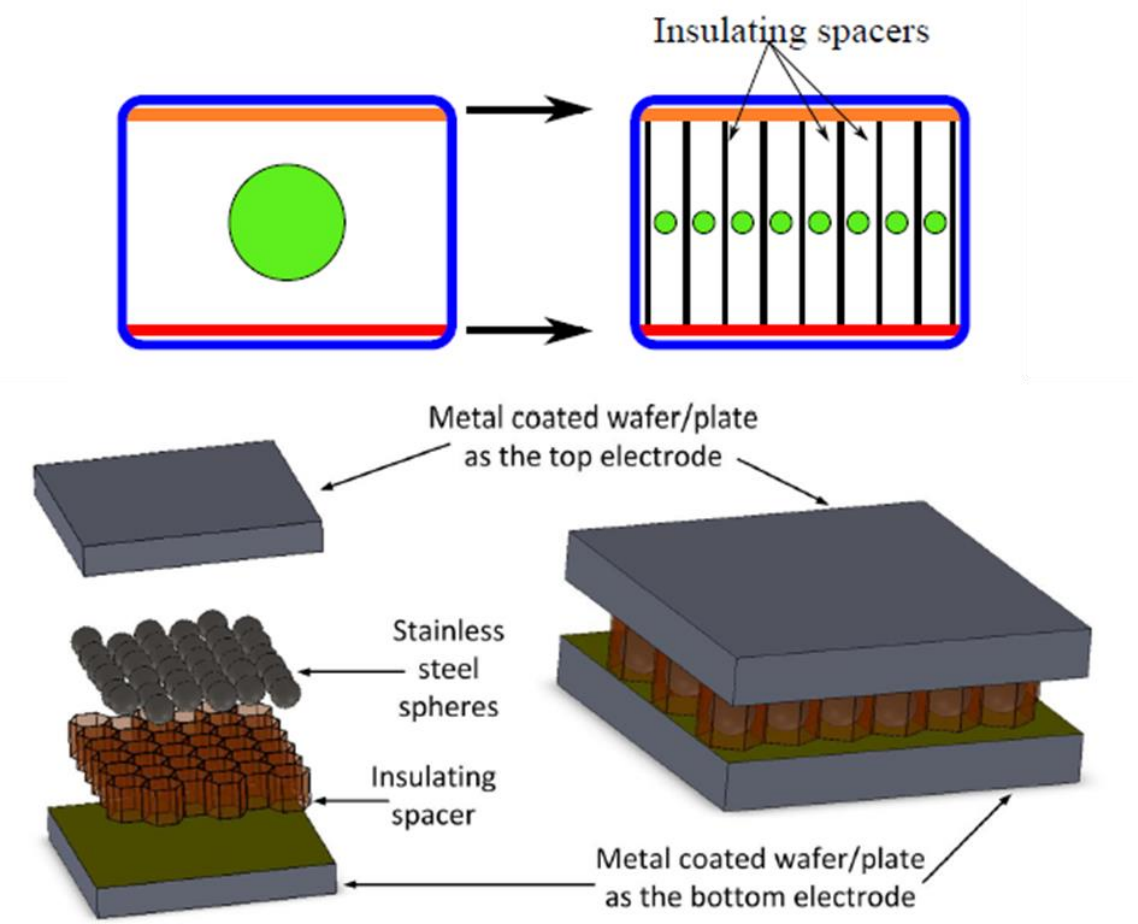


Figure 6.4: Summary of energy harvesting using material work-function difference. (a) Electrical and mechanical model of energy harvester based on material work-function difference. (b) Band diagram for two metal system before and after physical contact. (c) Electrical circuit diagram for energy harvester. (d) Difficulty with connecting capacitive energy harvesters in parallel.



S. Ardanuç et al., Middle East Technical University, 2012.

Figure 6.5: Schematic of charge shuttle based (contact) energy harvester using material work-function difference. Macroscale model for concept verification.

The vertical structure developed in this dissertation naturally lends itself to this application. The structure is intrinsically a charge shuttle (with the Channel electrically isolated) and the vertical design enables the highest density of devices. The main challenge is to have the proper orientation of metals for charge transfer via work-function difference. Additionally, operation at the resonant frequency of the device can be advantageous for high quality factor structures to enable large displacements. Therefore, the mass and stiffness of the pillars must be designed to

operate at frequencies that are common to vibration sources. These frequencies may be suited better by a microscale device.

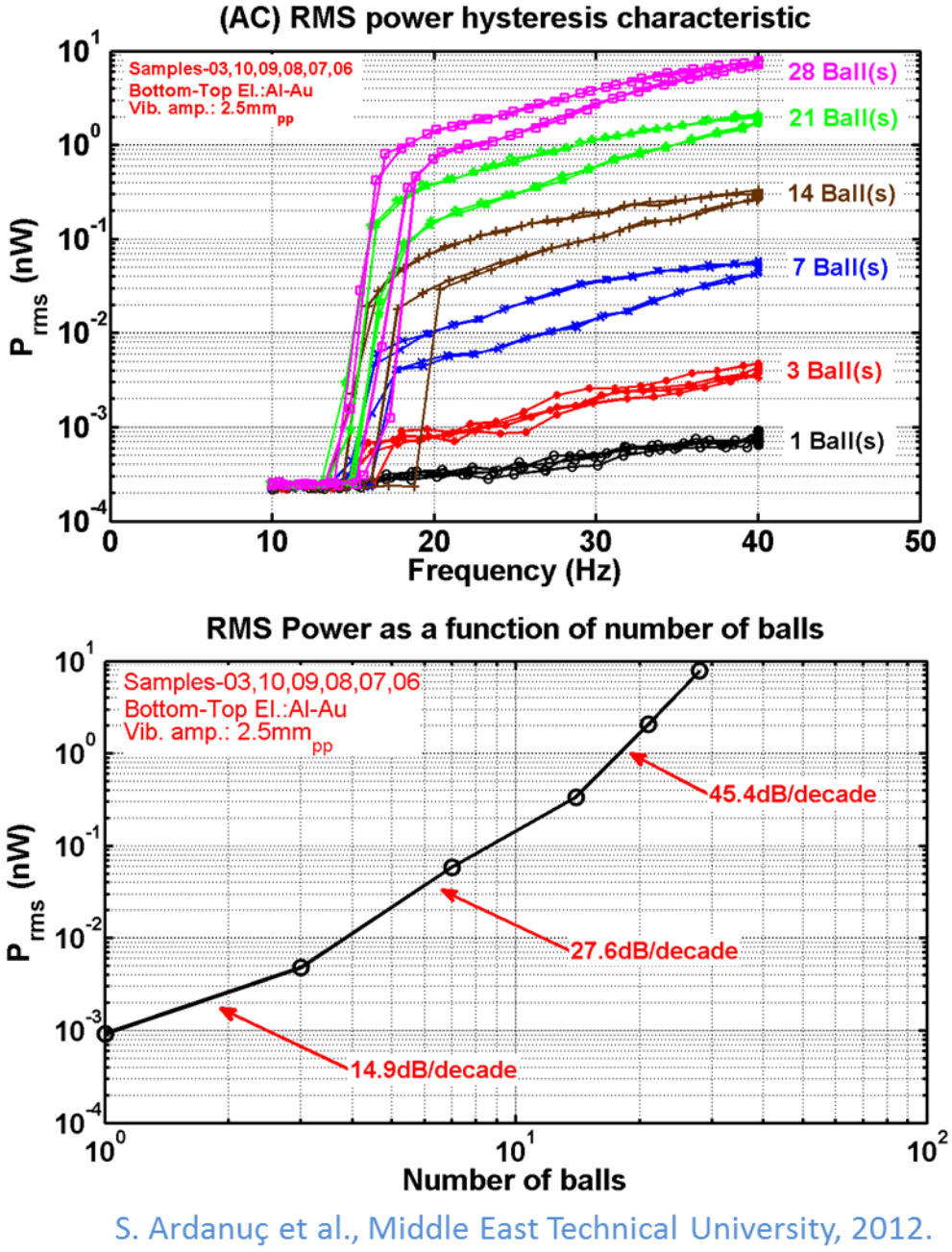


Figure 6.6: Electrical data for macroscale charge shuttle based on metal work function difference. Plots show RMS power generated by devices as a function of the number of metal balls.

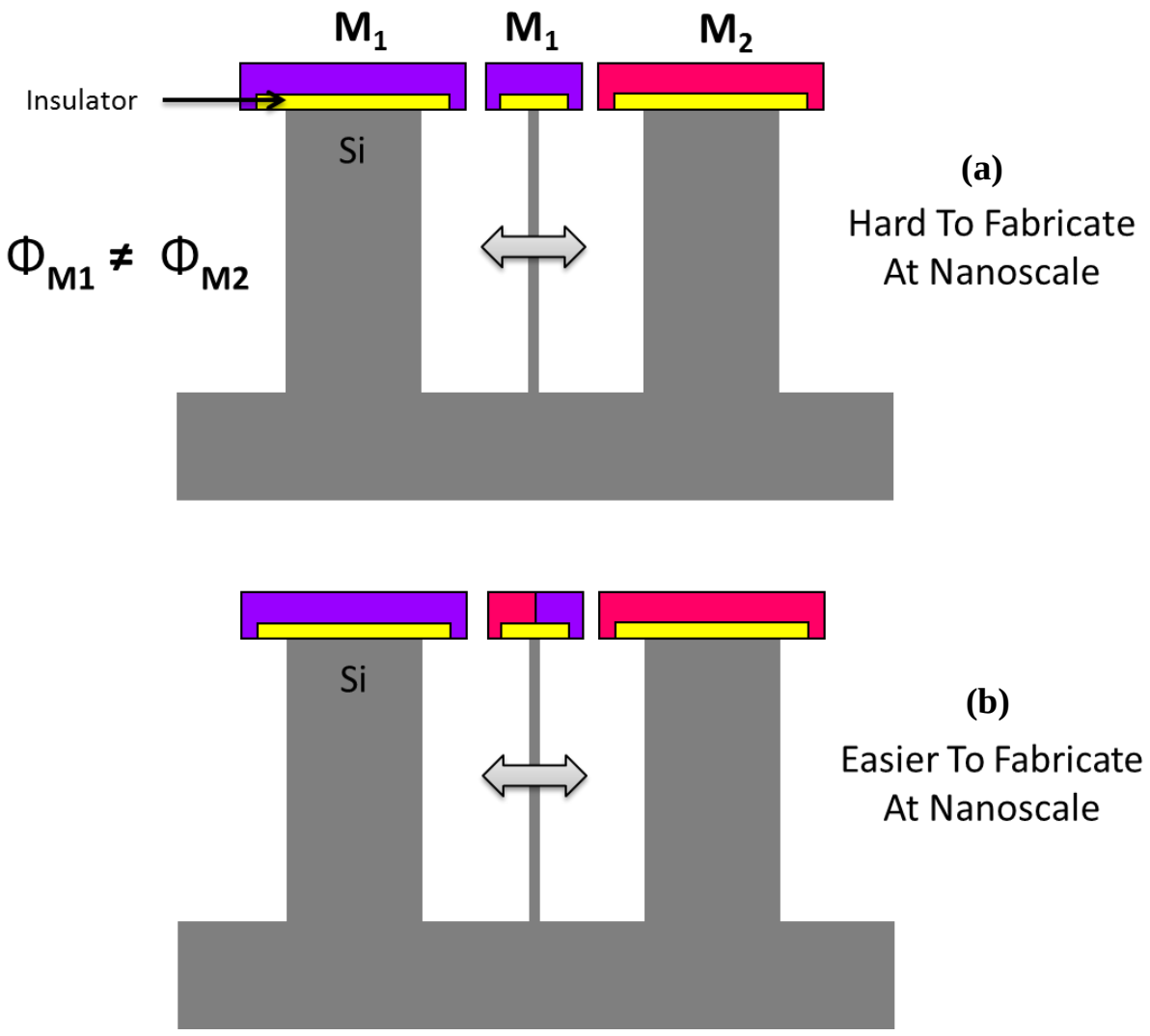


Figure 6.7: Top-down vertical charge shuttle energy harvester for nanoscale implementation. (a) Simple physical system for theoretical analysis. Complicated fabrication required. (b) Easy to fabricate two-metal charge shuttle.

A conceptually simple top-down vertical charge shuttle energy harvester can be seen in Figure 6.7(a). Only a single two-metal interface is used to create the built-in voltage for the device. However, such a design is difficult to realize in a nanoscale implementation. Defining two different metals in close proximity requires a significantly different fabrication method. Therefore, Figure 6.7(b) shows a similar design with alternating metal layers that can be accomplished by angled evaporation, as seen in Figure 6.8.

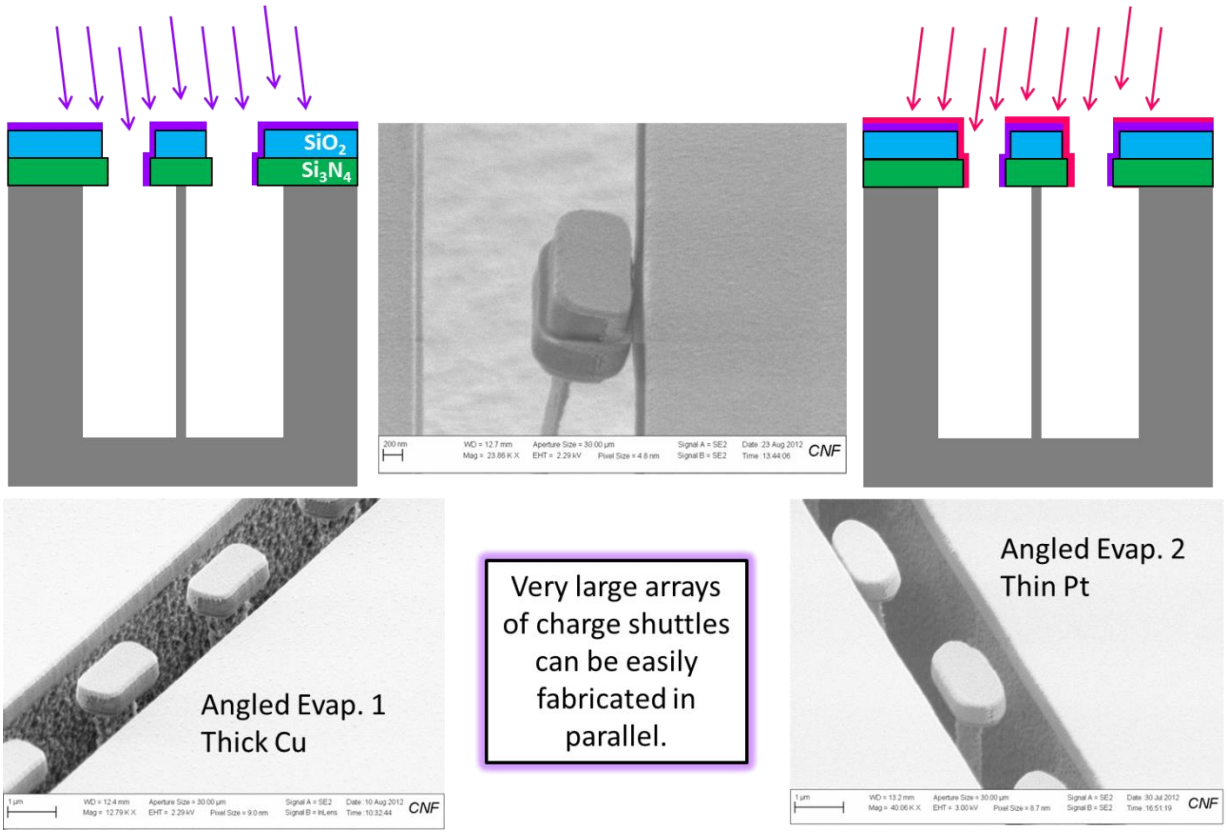


Figure 6.8: Simple top-down fabrication method for creating large arrays of two – metal charge shuttles.

The approach shown in Figure 6.8 can be used to create a charge shuttle with different metals on either side. Using two angled evaporations and a Channel (island) structure with a recessed top layer (SiO_2), the geometry can be such that the contacting surfaces are the materials of different work-function. This design can be used to make vast arrays of charge shuttle based energy harvesters. Although preliminary devices were fabricated, further development is needed for realization of this technology.

6.4 SENSING

Although nearly every MEMS/NEMS device that oscillates can be suggested for sensing applications, the vertical top-down design presented in this thesis offers particularly interesting qualities for sensing applications. Firstly, the compact vertical design enables extremely dense arrays of pillar based sensors, as seen in Figure 6.9. And secondly, particle deposition only occurs on only the top surface of the sensor, with the pillar protected by the Channel (island) structure. Looking at Figure 6.9(c), a typical planar sensor can have particles adhere anywhere along the length of the cantilever. MEMS/NEMS mechanical sensors use frequency shift to detect mass changes of the mechanical element. Additionally, the specific frequency shift will also be a function of position of the particle along the cantilever. Therefore, it is significantly more difficult to detect multiple particles on a single cantilever, or even to detect a single particle of any mass anywhere on a cantilever. Therefore, the vertical sensor design eliminates this difficulty and enables capacitive or optical sensing in an extremely compact form.

The work in this dissertation demonstrates a new class of structures that are not limited to use with switch-based applications. Many potential applications exist, including energy harvesting and sensing, to name a few. A compact versatile design using one or few lithographies has been shown to lend itself to numerous potential implementations and novel approaches to pre-existing and future applications.

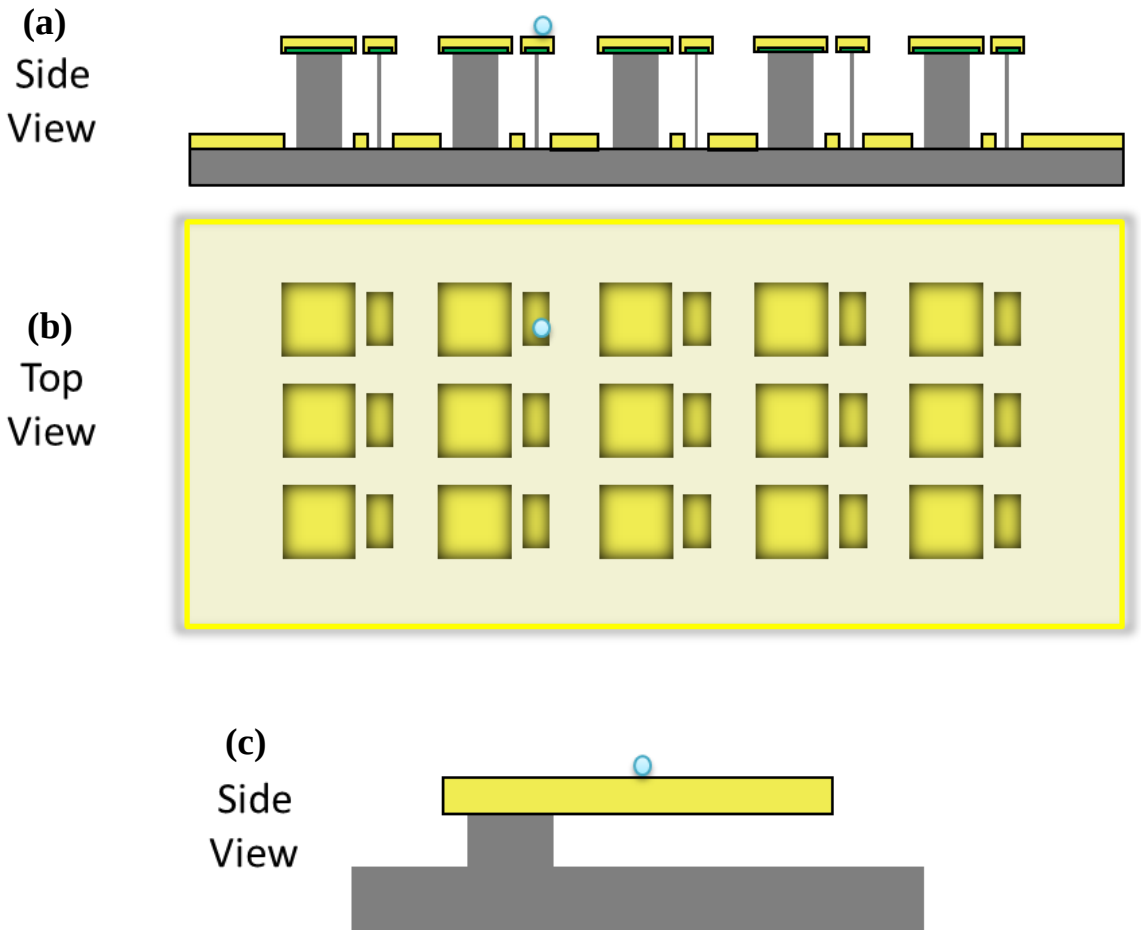


Figure 6.9: A vertical top-down sensor application. (a) Side view of an array of vertical top-down sensors. A round dot (representative of a particle to be detected) adheres to the top of the nano-pillar device. (b) Top view of an array of vertical sensors. Sensors can be read capacitively or optically. (c) Side view of typical planar sensor. Particles can deposit anywhere along the length of the cantilever, thereby making specific detection and counting of particles difficult due to the particle position dependence of the frequency shift.

BIBLIOGRAPHY

[1] J. Kim, S. Lee, J. Rubin, M. Kim, and S. Tiwari, "Scale changes in electronics: Implications for nanostructure devices for logic and memory and beyond," *Solid-State Electronics*, vol. 84, pp. 2–12, Jun. 2013.

[2] M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar, and K. Bernstein, "Scaling, power, and the future of CMOS," in *IEDM Technical Digest*, 2005, pp. 9–15.

[3] P. E. Ceruzzi, *A History of Modern Computing*, 2nd ed. Cambridge: The MIT Press, 2003.

[4] K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, and H. S. P. Wong, "Design Considerations for Complementary Nanoelectromechanical Logic Gates," in *IEDM Technical Digest*, 2007, pp. 299–302.

[5] M. Bao, *Analysis and Design Principles of MEMS Devices*. Amsterdam: Elsevier Science, 2005.

[6] J. I. Seeger and S. B. Crary, "Stabilization of electrostatically actuated mechanical devices," in *Proceedings of Transducers '97*, 1997, pp. 1133–1136.

[7] G. M. Rebeiz, *RF MEMS: Theory, Design, and Technology*, 1 edition. Hoboken: Wiley-Interscience, 2003.

[8] X. L. Feng, M. H. Matheny, C. A. Zorman, M. Mehregany, and M. L. Roukes, "Low Voltage Nanoelectromechanical Switches Based on Silicon Carbide Nanowires," *Nano Letters*, vol. 10, no. 8, pp. 2891–2896, Aug. 2010.

[9] M. W. Jang, C. L. Chen, W. E. Partlo, S. R. Patil, D. Lee, Z. Ye, D. Lilja, T. A. Taton, T. Cui, and S. A. Campbell, "A pure single-walled carbon nanotube thin film based three-terminal microelectromechanical switch," *Applied Physics Letters*, vol. 98, no. 7, p. 073502, Feb. 2011.

[10] H. H. Yang, J. O. Lee, and J. B. Yoon, "Maneuvering Pull-in Voltage of an Electrostatic Micro-switch by Introducing a Pre-charged Electrode," in *IEDM Technical Digest*, 2007, pp. 439–442.

[11] J. Yaung, L. Hutin, J. Jeon, and T. J. K. Liu, “Adhesive Force Characterization for MEM Logic Relays With Sub-Micron Contacting Regions,” *Journal of Microelectromechanical Systems*, vol. Early Access Online, 2013.

[12] Q. Ma, Q. Tran, T. K. A. Chou, J. Heck, H. Bar, R. Kant, and V. Rao, “Metal contact reliability of RF MEMS switches,” in *Proceedings of SPIE*, 2007, p. 646305.

[13] I. Laboriante, B. Bush, D. Lee, F. Liu, T. J. K. Liu, C. Carraro, and R. Maboudian, “Interfacial Adhesion between Rough Surfaces of Polycrystalline Silicon and Its Implications for M/NEMS Technology,” *Journal of Adhesion Science and Technology*, vol. 24, no. 15–16, pp. 2545–2556, 2010.

[14] O. Rezvanian, M. A. Zikry, C. Brown, and J. Krim, “Surface roughness, asperity contact and gold RF MEMS switch behavior,” *J. Micromech. Microeng.*, vol. 17, no. 10, p. 2006, Oct. 2007.

[15] B. D. Jensen, L. L.-W. Chow, K. Huang, K. Saitou, J. L. Volakis, and K. Kurabayashi, “Effect of nanoscale heating on electrical transport in RF MEMS switch contacts,” *Journal of Microelectromechanical Systems*, vol. 14, no. 5, pp. 935–946, 2005.

[16] B. Nikolić and P. B. Allen, “Electron transport through a circular constriction,” *Phys. Rev. B*, vol. 60, no. 6, pp. 3963–3969, Aug. 1999.

[17] L. L. W. Chow, S. A. Schrader, and K. Kurabayashi, “Transition from multiple to single microcontact conduction during hot switching of microelectromechanical switches with ball-shaped dimples,” *Applied Physics Letters*, vol. 89, no. 13, p. 133501, Sep. 2006.

[18] N. W. Ashcroft and N. D. Mermin, *Solid State Physics*, 1st ed. New York: Holt, Rinehart and Winston, 1976.

[19] P. M. T. M. van Attekum, P. H. Woerlee, G. C. Verkade, and A. A. M. Hoeben, “Influence of grain boundaries and surface Debye temperature on the electrical resistance of thin gold films,” *Phys. Rev. B*, vol. 29, no. 2, pp. 645–650, Jan. 1984.

[20] R. Holm, *Electric Contacts: Theory and Application*, 4th ed. New York: Springer-Verlag, 1967.

[21] S. Majumder, N. E. McGruer, G. G. Adams, P. M. Zavracky, R. H. Morrison, and J. Krim, "Study of contacts in an electrostatically actuated microswitch," *Sensors and Actuators A: Physical*, vol. 93, no. 1, pp. 19–26, Aug. 2001.

[22] T. J. K. Liu, J. Jeon, R. Nathanael, H. Kam, V. Pott, and E. Alon, "Prospects for MEM logic switch technology," in *IEDM Technical Digest*, 2010, pp. 18.3.1–18.3.4.

[23] R. Goggin, J.-E. Wong, B. Hecht, P. Fitzgerald, and M. Schirmer, "Fully integrated, high yielding, high reliability DC contact MEMS switch technology amp; control IC in standard plastic packages," in *IEEE Sensors Technical Digest*, 2011, pp. 958–961.

[24] W. W. Jang, J. O. Lee, J. B. Yoon, M. S. Kim, J. M. Lee, S. M. Kim, K. H. Cho, D. W. Kim, D. Park, and W.-S. Lee, "Fabrication and characterization of a nanoelectromechanical switch with 15-nm-thick suspension air gap," *Applied Physics Letters*, vol. 92, no. 10, p. 103110, Mar. 2008.

[25] O. Y. Loh and H. D. Espinosa, "Nanoelectromechanical contact switches," *Nat Nano*, vol. 7, no. 5, pp. 283–295, May 2012.

[26] P. Kim and C. M. Lieber, "Nanotube Nanotweezers," *Science*, vol. 286, no. 5447, pp. 2148–2150, Dec. 1999.

[27] Q. Li, S. M. Koo, H. D. Xiong, M. D. Edelstein, J. S. Suehle, X. Zhu, D. E. Ioannou, and C. A. Richter, "Methods to Characterize the Electrical and Mechanical Properties of Si Nanowires," in *AIP Conference Proceedings*, 2007, pp. 457–461.

[28] W. Kwon, J. Jeon, L. Hutin, and T. J. K. Liu, "Electromechanical Diode Cell for Cross-Point Nonvolatile Memory Arrays," *IEEE Electron Device Letters*, vol. 33, no. 2, pp. 131–133, 2012.

[29] C. Chen, R. Parsa, N. Patil, S. Chong, K. Akarvardar, J. Provine, D. Lewis, J. Watt, R. T. Howe, H. S. P. Wong, and S. Mitra, "Efficient FPGAs using nanoelectromechanical relays," in *Proceedings of the 18th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, 2010, pp. 273–282.

[30] H. R. Shea, "Effects of radiation on MEMS," in *Proceedings of SPIE*, 2011, p. 79280E.

[31] T. H. Lee, S. Bhunia, and M. Mehregany, "Electromechanical Computing at 500°C with Silicon Carbide," *Science*, vol. 329, no. 5997, pp. 1316–1318, Sep. 2010.

[32] T.-J. K. Liu, L. Hutin, I. R. Chen, R. Nathanael, Y. Chen, M. Spencer, and E. Alon, "Recent progress and challenges for relay logic switch technology," in *Symposium on VLSI Technology (VLSIT) Digest*, 2012, pp. 43–44.

[33] H. Kam, T. J. K. Liu, V. Stojanović, D. Markovic, and E. Alon, "Design, Optimization, and Scaling of MEM Relays for Ultra-Low-Power Digital Logic," *IEEE Transactions on Electron Devices*, vol. 58, no. 1, pp. 236–250, 2011.

[34] D. Grogg, Y. Pu, A. Knoll, U. Duerig, U. Drechsler, C. Hagleitner, and M. Despont, "NEM switch technologies for low-power logic applications," in *IEEE Sensors Technical Digest*, 2012, pp. 1–3.

[35] G. Rubio-Bollinger, S. R. Bahn, N. Agraït, K. W. Jacobsen, and S. Vieira, "Mechanical Properties and Formation Mechanisms of a Wire of Single Gold Atoms," *Phys. Rev. Lett.*, vol. 87, no. 2, p. 026101, Jun. 2001.

[36] H. Kwon, D. J. Choi, J. H. Park, H. C. Lee, Y. H. Park, Y. D. Kim, H. J. Nam, Y. C. Joo, and J. U. Bu, "Contact materials and reliability for high power RF-MEMS switches," in *Proceedings of 20th IEEE International Conference on MEMS*, 2007, pp. 231–234.

[37] A. Fruehling, S. Xiao, M. Qi, K. Roy, and D. Peroulis, "Nano-switch for study of gold contact behavior," in *IEEE Sensors Technical Digest*, 2009, pp. 248–251.

[38] M. B. Henry and L. Nazhandali, "NEMS-Based Functional Unit Power-Gating: Design, Analysis, and Optimization," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 2, pp. 290–302, 2013.

[39] B. Halg, "On a micro-electro-mechanical nonvolatile memory cell," *IEEE Transactions on Electron Devices*, vol. 37, no. 10, pp. 2230–2236, 1990.

[40] Y. Tsuchiya, K. Takai, N. Momo, T. Nagami, H. Mizuta, S. Oda, S. Yamaguchi, and T. Shimada, "Nanoelectromechanical nonvolatile memory device incorporating nanocrystalline Si dots," *Journal of Applied Physics*, vol. 100, no. 9, p. 094306, Nov. 2006.

[41] V. Pott, G. L. Chua, R. Vaddi, J. M. L. Tsai, and T. T. Kim, "The Shuttle Nanoelectromechanical Nonvolatile Memory," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 1137–1143, 2012.

[42] M. Liu, H. Yang, S. Tanachutiwat, and W. Wang, "FPGA based on integration of carbon nanorelays and CMOS devices," in *Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures*, 2009, pp. 61–64.

[43] M. Lapisa, G. Stemme, and F. Niklaus, "Wafer-Level Heterogeneous Integration for MOEMS, MEMS, and NEMS," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 17, no. 3, pp. 629–644, 2011.

[44] G. K. Fedder, R. T. Howe, T. J. K. Liu, and E. P. Quevy, "Technologies for Cofabricating MEMS and Electronics," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 306–322, 2008.

[45] D. R. Collins, J. B. Sampsell, L. J. Hornbeck, J. M. Florence, P. A. Penz, and M. T. Gately, "Deformable mirror device spatial light modulators and their applicability to optical neural networks," *Appl. Opt.*, vol. 28, no. 22, pp. 4900–4907, Nov. 1989.

[46] H. Takeuchi, A. Wung, X. Sun, R. T. Howe, and T. J. King, "Thermal budget limits of quarter-micrometer foundry CMOS for post-processing MEMS devices," *IEEE Transactions on Electron Devices*, vol. 52, no. 9, pp. 2081–2086, 2005.

[47] B. Li, B. Xiong, L. Jiang, Y. Zohar, and M. Wong, "Germanium as a versatile material for low-temperature micromachining," *Journal of Microelectromechanical Systems*, vol. 8, no. 4, pp. 366–372, 1999.

[48] S. Sedky, P. Fiorini, M. Caymax, A. Verbist, and C. Baert, "Thermally insulated structures for IR bolometers, made of polycrystalline silicon germanium alloys," in *Proceedings of International Conference on Solid State Sensors and Actuators*, 1997, vol. 1, pp. 237–240 vol.1.

[49] A. E. Franke, D. Bilic, D. T. Chang, P. T. Jones, T. J. King, R. T. Howe, and G. C. Johnson, "Post-CMOS integration of germanium microstructures," in *Proceedings of 12th IEEE International Conference on MEMS*, 1999, pp. 630–637.

[50] A. Witvrouw, "CMOS-MEMS integration: why, how and what?," in *Proceedings of the 2006 IEEE/ACM International Conference on Computer-Aided Design*, New York, NY, USA, 2006, pp. 826–827.

[51] G. M. Rebeiz, "RF MEMS switches: status of the technology," in *12th IEEE International Conference on Solid-State Sensors, Actuators and Microsystems*, 2003, vol. 2, pp. 1726–1729 vol.2.

[52] P. Ekkels, X. Rottenberg, R. Puers, and H. a. C. Tilmans, “Evaluation of platinum as a structural thin film material for RF-MEMS devices,” *J. Micromech. Microeng.*, vol. 19, no. 6, p. 065010, Jun. 2009.

[53] R. Parsa, M. Shavezipur, W. S. Lee, S. Chong, D. Lee, H. S. P. Wong, R. Maboudian, and R. T. Howe, “Nanoelectromechanical relays with decoupled electrode and suspension,” in *Proceedings of IEEE 24th International Conference on MEMS*, 2011, pp. 1361–1364.

[54] H. F. Dadgour, M. M. Hussain, C. Smith, and K. Banerjee, “Design and analysis of compact ultra Energy-Efficient logic gates using laterally-actuated double-electrode NEMS,” in *Proceedings of 47th ACM/IEEE DAC Conference*, 2010, pp. 893–896.

[55] M. Spencer, F. Chen, C. C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T. J. K. Liu, D. Markovic, E. Alon, and V. Stojanovic, “Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Applications,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 308–320, 2011.

[56] W. Xiang and C. Lee, “Nanoelectromechanical torsion switch of low operation voltage for nonvolatile memory application,” *Applied Physics Letters*, vol. 96, no. 19, pp. 193113–193113–3, May 2010.

[57] P. Yang, “The Chemistry and Physics of Semiconductor Nanowires,” *MRS Bulletin*, vol. 30, no. 02, pp. 85–91, 2005.

[58] S. Axelsson, E. E. B. Campbell, L. M. Jonsson, J. Kinaret, S. W. Lee, Y. W. Park, and M. Sveningsson, “Theoretical and experimental investigations of three-terminal carbon nanotube relays,” *New J. Phys.*, vol. 7, no. 1, p. 245, Nov. 2005.

[59] J. E. Jang, S. N. Cha, Y. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim, “Nanoelectromechanical switches with vertically aligned carbon nanotubes,” *Applied Physics Letters*, vol. 87, no. 16, pp. 163114–163114–3, Oct. 2005.

[60] C. Li and T. W. Chou, “A structural mechanics approach for the analysis of carbon nanotubes,” *International Journal of Solids and Structures*, vol. 40, no. 10, pp. 2487–2499, May 2003.

[61] E. W. Wong, P. E. Sheehan, and C. M. Lieber, “Nanobeam Mechanics: Elasticity, Strength, and Toughness of Nanorods and Nanotubes,” *Science*, vol. 277, no. 5334, pp. 1971–1975, Sep. 1997.

[62] M. A. Hopcroft, W. D. Nix, and T. W. Kenny, "What is the Young's Modulus of Silicon?," *Journal of Microelectromechanical Systems*, vol. 19, no. 2, pp. 229–238, 2010.

[63] J. Rubin, R. Sundararaman, M. Kim, and S. Tiwari, "A Low-Voltage Torsion Nanorelay," *IEEE Electron Device Letters*, vol. 32, no. 3, pp. 414–416, 2011.

[64] R. Legtenberg, A. W. Groeneveld, and M. Elwenspoek, "Comb-drive actuators for large displacements," *J. Micromech. Microeng.*, vol. 6, no. 3, p. 320, Sep. 1996.

[65] D. R. Koenig and E. M. Weig, "Voltage-sustained self-oscillation of a nano-mechanical electron shuttle," *Applied Physics Letters*, vol. 101, no. 21, pp. 213111–213111–5, Nov. 2012.

[66] M. A. Beunder, R. Van Kampen, D. Lacey, M. Renault, and C. G. Smith, "A new embedded NVM technology for low-power, high temperature, rad-hard applications," in *Proceedings of Non-Volatile Memory Technology Symposium*, 2005, pp. 65–68.

[67] K. Cai, M. Müller, J. Bossert, A. Rechtenbach, and K. D. Jandt, "Surface structure and composition of flat titanium thin films as a function of film thickness and evaporation rate," *Applied Surface Science*, vol. 250, no. 1–4, pp. 252–267, Aug. 2005.

[68] C. Gustin, L. H. A. Leunissen, A. Mercha, S. Decoutere, and G. Lorusso, "Impact of line width roughness on the matching performances of next-generation devices," *Thin Solid Films*, vol. 516, no. 11, pp. 3690–3696, Apr. 2008.

[69] L. Kogut and K. Komvopoulos, "Electrical contact resistance theory for conductive rough surfaces," *Journal of Applied Physics*, vol. 94, no. 5, pp. 3153–3162, Sep. 2003.

[70] M. W. Kim, Y. H. Song, H. H. Yang, and J. B. Yoon, "An ultra-low voltage MEMS switch using stiction-recovery actuation," *J. Micromech. Microeng.*, vol. 23, no. 4, p. 045022, Apr. 2013.

[71] AZoM.com Staff Writers, "Deep Silicon Etch Applications in MEMS and NEMS," 31-Jul-2013. [Online]. Available: www.azom.com/article.aspx?ArticleID=9742. [Accessed: 22-Aug-2013].

[72] K. Mohamed and M. M. Alkaisi, "The Fabrication of High Aspect Ratio Nanostructures on Quartz Substrate," in *Updates in Advanced Lithography*, S. Hosaka, Ed. InTech, 2013.

[73] K. E. Petersen, “Dynamic micromechanics on silicon: Techniques and devices,” *IEEE Transactions on Electron Devices*, vol. 25, no. 10, pp. 1241–1250, 1978.

[74] H. Ogawa, K. Suzuki, S. Kaneko, Y. Nakano, Y. Ishikawa, and T. Kitahara, “Measurements of mechanical properties of microfabricated thin films,” in *Proceedings of IEEE 10th International Workshop on MEMS*, 1997, pp. 430–435.

[75] E. R. Parker, B. J. Thibeault, M. F. Aimi, M. P. Rao, and N. C. MacDonald, “Inductively Coupled Plasma Etching of Bulk Titanium for MEMS Applications,” *J. Electrochem. Soc.*, vol. 152, no. 10, pp. C675–C683, Oct. 2005.

[76] J. A. Thornton and D. W. Hoffman, “Stress-related effects in thin films,” *Thin Solid Films*, vol. 171, no. 1, pp. 5–31, Apr. 1989.

[77] L. Zhang, H. Yang, X. Pang, K. Gao, and A. A. Volinsky, “Microstructure, residual stress, and fracture of sputtered TiN films,” *Surface and Coatings Technology*, vol. 224, pp. 120–125, Jun. 2013.

[78] X. Li, T. Ono, Y. Wang, and M. Esashi, “Ultrathin single-crystalline-silicon cantilever resonators: Fabrication technology and significant specimen size effect on Young’s modulus,” *Applied Physics Letters*, vol. 83, no. 15, pp. 3081–3083, 2003.

[79] R. E. Rudd and J. Q. Broughton, “Atomistic simulation of MEMS resonators through the coupling of length scales,” *J. Model Simul. Microsyst.*, vol. 1, no. 29, pp. 29–38, 1999.

[80] S. Lai, R. Westerman, D. Purser, M. DeVre, D. Johnson, and D. Lishan, “Advances in deep silicon etching.” [Online]. Available: http://www.plasmatherm.com/korean/pdfs/papers/4.%20Advances%20in%20Deep%20Silicon%20Etching.pdf. [Accessed: 22-Aug-2013].

[81] J. E. Jang, S. N. Cha, Y. J. Choi, D. J. Kang, T. P. Butler, D. G. Hasko, J. E. Jung, J. M. Kim, and G. A. J. Amaratunga, “Nanoscale memory cell based on a nanoelectromechanical switched capacitor,” *Nat Nano*, vol. 3, no. 1, pp. 26–30, Jan. 2008.

[82] B. Bhushan, “Adhesion and stiction: Mechanisms, measurement techniques, and methods for reduction,” *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 21, no. 6, pp. 2262–2296, 2003.

[83] D. W. Hess, "Plasma-assisted oxidation, anodization, and nitridation of silicon," *IBM Journal of Research and Development*, vol. 43, no. 1.2, pp. 127–145, 1999.

[84] K.-Y. Chiu, J. L. Moll, and J. Manoliu, "A Bird's Beak Free Local Oxidation Technology Feasible for VLSI Circuits Fabrication," *IEEE Journal of Solid-State Circuits*, vol. 17, no. 2, pp. 166–170, 1982.

[85] H. I. Liu, D. K. Biegelsen, F. A. Ponce, N. M. Johnson, and R. F. W. Pease, "Self-limiting oxidation for fabricating sub-5 nm silicon nanowires," *Applied Physics Letters*, vol. 64, no. 11, pp. 1383–1385, Mar. 1994.

[86] H. Robbins and B. Schwartz, "Chemical Etching of Silicon I. The System HF, HNO3 and H2O," *J. Electrochem. Soc.*, vol. 106, no. 6, pp. 505–508, Jun. 1959.

[87] K. R. Williams and R. S. Muller, "Etch rates for micromachining processing," *Journal of Microelectromechanical Systems*, vol. 5, no. 4, pp. 256–269, 1996.

[88] A. A. Hamzah, N. Abd Aziz, B. Yeop Majlis, J. Yunas, C. F. Dee, and B. Bais, "Optimization of HNA etching parameters to produce high aspect ratio solid silicon microneedles," *Journal of Micromechanics and Microengineering*, vol. 22, no. 9, p. 095017, Sep. 2012.

[89] J. W. Coburn and H. F. Winters, "Ion- and electron-assisted gas-surface chemistry—An important effect in plasma etching," *Journal of Applied Physics*, vol. 50, no. 5, pp. 3189–3196, May 1979.

[90] R. P. Manginell, G. C. Frye-Mason, W. K. Schubert, R. J. Shul, and C. G. Willison, "Microfabrication of Membrane-Based Devices by Deep-Reactive Ion Etching (DRIE) of Silicon," in *Proceedings of the Electrochemical Society Meeting*, 1998.

[91] K. R. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing-Part II," *Journal of Microelectromechanical Systems*, vol. 12, no. 6, pp. 761–778, 2003.

[92] W. J. Arora, A. J. Nichol, H. I. Smith, and G. Barbastathis, "Membrane folding to achieve three-dimensional nanostructures: Nanopatterned silicon nitride folded with stressed chromium hinges," *Applied Physics Letters*, vol. 88, no. 5, p. 053108, Jan. 2006.

[93] G. Harvey, "Cyantek Corporation Material Safety Data Sheet CR-14S," 23-Mar-2012. [Online]. Available: http://mnm.physics.mcgill.ca/system/files/CR-14S_MSDS.pdf. [Accessed: 22-Aug-2013].

[94] "RIE Reactive Ion Etching," *Oxford Instruments*. [Online]. Available: http://www.oxfordplasma.de/technols/rie.htm. [Accessed: 22-Aug-2013].

[95] "RIE - ICP (helical) Inductive Coupled Plasma," *Oxford Instruments*. [Online]. Available: http://www.oxfordplasma.de/technols/rie_icp.htm. [Accessed: 22-Aug-2013].

[96] A. M. Hynes, H. Ashraf, J. K. Bhardwaj, J. Hopkins, I. Johnston, and J. N. Shepherd, "Recent advances in silicon etching for MEMS using the ASE^{TM} process," *Sensors and Actuators A: Physical*, vol. 74, no. 1–3, pp. 13–17, Apr. 1999.

[97] B. R. Ilic, S. Krylov, M. Kondratovich, and H. G. Craighead, "Optically Actuated Nanoelectromechanical Oscillators," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 13, no. 2, pp. 392–399, 2007.

[98] A. Bosseboeuf, C. Bréluzeau, F. Parrain, P. Coste, J.-P. Gilles, S. Megherbi, and X. Le Roux, "In-plane vibration measurement of microdevices by the knife-edge technique in reflection mode," in *Proceedings of SPIE*, Ancona, Italy, 2006, vol. 6345, p. 63451D.

[99] C. Rembe, R. Kant, and R. S. Muller, "Optical measurement methods to study dynamic behavior in MEMS," 2001, vol. 4400, pp. 127–137.

[100] D. Karabacak, T. Kouh, C. C. Huang, and K. L. Ekinci, "Optical knife-edge technique for nanomechanical displacement detection," *Applied Physics Letters*, vol. 88, no. 19, pp. 193122–193122–3, 2006.

[101] G. J. McShane, M. Boutchich, A. S. Phani, D. F. Moore, and T. J. Lu, "Young's modulus measurement of thin-film materials using micro-cantilevers," *J. Micromech. Microeng.*, vol. 16, no. 10, p. 1926, Oct. 2006.

[102] S. B. Coskun, M. T. Atay, and B. Ozturk, "Transverse Vibration Analysis of Euler-Bernoulli Beams Using Analytical Approximate Techniques," in *Advances in Vibration Anaylsis Research*, InTech, 2011.

[103] X. Mellhaoui, R. Dussart, T. Tillocher, P. Lefaucheux, P. Ranson, M. Boufnichel, and L. J. Overzet, "SiOxFy passivation layer in silicon cryoetching," *Journal of Applied Physics*, vol. 98, no. 10, pp. 104901–104901–10, Nov. 2005.

[104] M. J. Walker, "Comparison of Bosch and cryogenic processes for patterning high-aspect-ratio features in silicon," in *Proceedings of SPIE*, 2001, vol. 4407, pp. 89–99.

[105] V. Jovanović, T. Suligoj, P. Biljanović, and L. K. Nanver, "FinFET technology for wide-channel devices with ultra-thin silicon body," in *Proceedings of the 31st International Convention MIPRO*, 2008, pp. 79–83.

[106] S. Jensen and O. Hansen, "Characterization of the microloading effect in deep reactive ion etching of silicon," in *Proceedings of SPIE*, 2004, vol. 5342, pp. 111–118.

[107] K. Kuehl, S. Vogel, U. Schaber, R. Schafflik, and B. Hillerich, "Advanced silicon trench etching in MEMS applications," in *Proceedings of SPIE*, 1998, vol. 3511, pp. 97–105.

[108] "High-Density Radical Flux (HDRF)," *Nanoplas*. [Online]. Available: http://www.nanoplas.eu/en/technologies/hdrf/. [Accessed: 22-Aug-2013].

[109] L. . Vergara, M. C. . Passeggi Jr., and J. Ferrón, "The role of passivation in titanium oxidation: thin film and temperature effects," *Applied Surface Science*, vol. 187, no. 3–4, pp. 199–206, Feb. 2002.

[110] S. Springer and P. E. Schmid, "Free carriers in nanocrystalline titanium dioxide thin films," Ecole polytechnique fédérale de Lausanne, Lausanne, Switzerland, 2004.

[111] S. A. Campbell, H. S. Kim, D. C. Gilmer, B. He, T. Ma, and W. L. Gladfelter, "Titanium dioxide (TiO2)-based gate insulators," *IBM Journal of Research and Development*, vol. 43, no. 3, pp. 383–392, 1999.

[112] H. Lee, R. A. Coutu, S. Mall, and K. D. Leedy, "Characterization of metal and metal alloy films as contact materials in MEMS switches," *J. Micromech. Microeng.*, vol. 16, no. 3, p. 557, Mar. 2006.

[113] P. Garrou, C. Bower, and P. Ramm, *Handbook of 3D integration: technology and applications of 3D integrated circuits*. Weinheim, Germany: Wiley-VCH Verlag, 2008.

[114] C.-T. Ko and K.-N. Chen, "Wafer-level bonding/stacking technology for 3D integration," *Microelectronics Reliability*, vol. 50, no. 4, pp. 481–488, Apr. 2010.

[115] E. F. Pabo, "Enabling Technologies for 3D Integration: Aligned Permanent Bonding and Temporary Bonding," presented at the 3D System Integration Workshop, Georgia Tech, 13-Jun-2011.

[116] V. Lindroos, M. Tilli, A. Lehto, and T. Motooka, *Handbook of Silicon Based MEMS Materials and Technologies*, 1st ed. Boston: William Andrew Publishing, 2010.

[117] Z. Liu and D. L. DeVoe, "Micromechanism fabrication using silicon fusion bonding," *Robotics and Computer-Integrated Manufacturing*, vol. 17, no. 1–2, pp. 131–137, Feb. 2001.

[118] R. Chanchani, "3D Integration Technologies - An Overview," in *Materials for Advanced Packaging*, Springer-Verlag, 2009, pp. 1–50.

[119] A. Yu, J. H. Lau, S. W. Ho, A. Kumar, H. W. Yin, J. M. Ching, V. Kripesh, D. Pinjala, S. Chen, C.-F. Chan, C.-C. Chao, S. Chiu, C.-M. Huang, and C. Chen, "Three dimensional interconnects with high aspect ratio TSVs and fine pitch solder microbumps," in *Proceedings of 59th Electronic Components and Technology Conference*, 2009, pp. 350–354.

[120] P. Gueguen, L. Di Cioccio, M. Rivoire, D. Scevola, M. Zussy, A. Ma. Charvet, L. Bally, D. Lafond, and L. Clavelier, "Copper direct bonding for 3D integration," in *Proceedings of the Interconnect Technology Conference*, 2008, pp. 61–63.

[121] M. A. Schmidt, "Wafer-to-wafer bonding for microstructure formation," *Proceedings of the IEEE*, vol. 86, no. 8, pp. 1575–1585, 1998.

[122] F. Niklaus, M. Lapisa, S. J. Bleiker, V. Dubois, N. Roxhed, A. C. Fischer, F. Forsberg, G. Stemme, D. Grogg, and M. Despont, "Wafer-level heterogeneous 3D integration for MEMS and NEMS," in *Proceedings of the 3rd IEEE International Workshop on Low Temperature Bonding for 3D Integration (LTB-3D)*, 2012, pp. 247–252.

[123] S. Kühne and C. Hierold, "Wafer-level packaging and direct interconnection technology based on hybrid bonding and through silicon vias," *J. Micromech. Microeng.*, vol. 21, no. 8, p. 085032, Aug. 2011.

[124] M. Despont, U. Drechsler, R. Yu, H. B. Pogge, and P. Vettiger, "Wafer-scale microdevice transfer/interconnect: its application in an AFM-based data-storage system," *Journal of Microelectromechanical Systems*, vol. 13, no. 6, pp. 895–901, 2004.

[125] J. W. P. Chen and R. T. Howe, "Wafer reconstitution with precision dry front-to-front registration," in *Proceedings of the Solid-State Sensors, Actuators and Microsystems Conference*, 2009, pp. 1095–1098.

[126] C. Welch, "Nanoscale Etching in Inductively Coupled Plasmas." Oxford Instruments, 2011.

[127] C. J. D. Craigie, T. Sheehan, V. N. Johnson, S. L. Burkett, A. J. Moll, and W. B. Knowlton, "Polymer thickness effects on Bosch etch profiles," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 20, no. 6, pp. 2229–2232, 2002.

[128] V. Dragoi, E. Pabo, J. Burggraf, and G. Mittendorfer, "CMOS: compatible wafer bonding for MEMS and wafer-level 3D integration," *Microsyst Technol*, vol. 18, no. 7–8, pp. 1065–1075, Aug. 2012.

[129] R. Nadipalli, J. Fan, K. H. Li, K. H. Wee, H. Yu, and C. S. Tan, "3D integration of MEMS and CMOS via Cu-Cu bonding with simultaneous formation of electrical, mechanical and hermetic bonds," in *Proceedings of the 3D Systems Integration Conference (3DIC)*, 2012, pp. 1–5.

[130] I. Kuehne, A. Frey, D. Marinkovic, G. Eckstein, and H. Seidel, "Power MEMS—A capacitive vibration-to-electrical energy converter with built-in voltage," *Sensors and Actuators A: Physical*, vol. 142, no. 1, pp. 263–269, Mar. 2008.

[131] S. M. Ardanuc, O. Zorlu, H. Kulah, and T. Akin, "Method of energy harvesting using built-in potential difference of metal-to-metal junctions and device thereof," WO2013115733 A108-Aug-2013.

[132] S. Ardanuc¸, "A Charge Shuttle Device for Vibration Harvesting Using Built-in Potential Difference of Metal-to-Metal Junctions: Modeling, Simulations, and Experiments," Middle East Technical University, Ankara, Turkey, Nov. 2011.